EXHIBIT A

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

WI-LAN INC.,	§	
	§	
Plaintiff,	§	
	§	**C.A. No. _____**
v.	§	
	§	**JURY TRIAL DEMANDED**
SHARP CORPORATION and	§	
	§	
SHARP ELECTRONICS CORPORATION,	§	
	§	
	§	
Defendants.	§	
	§	

PLAINTIFF'S COMPLAINT

Plaintiff Wi-LAN Inc., by and through its undersigned counsel, files this Complaint for Patent Infringement against Defendants Sharp Corporation and Sharp Electronics Corporation (collectively, "Sharp").

THE PARTIES

1. Plaintiff Wi-LAN Inc. ("Wi-LAN") is a corporation formed under the laws of the country of Canada with its principal place of business at 303 Terry Fox Drive, Suite 300, Ottawa, Ontario, Canada, K2K 3J1. Wi-LAN is a leading technology innovation and licensing business actively engaged in research, development, and licensing of new technologies.

2. Upon information and belief, Sharp Corporation is a company incorporated in Japan located at 22-22 Negaikecho, Abeno-Ku, Osaka 545-8522, Japan. Upon information and belief, Sharp Corporation may be served with process in Japan pursuant to the Hague Convention on the Service Abroad of Judicial and Extrajudicial Documents in Civil or Commercial Matters.

3. Upon information and belief, Sharp Electronics Corporation ("Sharp Electronics") is a New York corporation headquartered at Sharp Plaza, Mahwah, New Jersey 07430. Upon information and belief, Sharp Electronics may be served with process by serving its registered agent, C T Corporation System, 111 Eighth Avenue, New York, New York 10011.

4. Upon information and belief, Sharp Corporation is the parent of Sharp Electronics.

5. Upon information and belief, Sharp has conducted and regularly conducts business within this District, has purposefully availed itself of the privileges of conducting business in this District, and has sought protection and benefit from the laws of the State of Delaware.

JURISDICTION AND VENUE

6. This action arises under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq.*, including 35 U.S.C. §§ 271, 281, 283, 284, and 285. This Court has subject matter jurisdiction over this case for patent infringement under 28 U.S.C. §§ 1331 and 1338(a).

7. As further detailed herein, this Court has personal jurisdiction over Sharp Electronics. Sharp Electronics is amenable to service of summons for this action. Furthermore, personal jurisdiction over Sharp Electronics in this action comports with due process. Sharp America has conducted and regularly conducts business within the United States and this District. Sharp America has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in Delaware and this District. Sharp Electronics has sought protection and benefit from the laws of the State of Delaware by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

8. Sharp Electronics – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – ships, distributes, offers for sale, and/or sells its products in the United States and this District. Sharp Electronics has purposefully and voluntarily placed one or more of its infringing products, as described below, into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. Sharp Electronics knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, Sharp Electronics has committed the tort of patent infringement in this District and/or has induced others to commit patent infringement in this District. Plaintiff's cause of action for patent infringement arises directly from Sharp Electronics' activities in this District.

9. As further detailed herein, this Court has personal jurisdiction over Sharp Corporation. Sharp Corporation is amenable to service of summons for this action. Furthermore, personal jurisdiction over Sharp Corporation in this action comports with due process. Sharp Corporation has conducted and regularly conducts business within the United States and this District. Sharp Corporation has purposefully availed itself of the privileges of conducting business in the United States, and more specifically in Delaware and this District. Sharp Corporation has sought protection and benefit from the laws of the State of Delaware by maintaining offices of its United States subsidiaries in Delaware and/or by placing infringing products into the stream of commerce through an established distribution channel with the awareness and/or intent that they will be purchased by consumers in this District.

10. Sharp Corporation – directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents – ships, distributes, offers for sale,

and/or sells its products in the United States and this District. Sharp Corporation has purposefully and voluntarily placed one or more of its infringing products, as described below, into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. Sharp Corporation knowingly and purposefully ships infringing products into and within this District through an established distribution channel. These infringing products have been and continue to be purchased by consumers in this District. Upon information and belief, through those activities, Sharp Corporation has committed the tort of patent infringement in this District and/or has induced others to commit patent infringement in this District. Plaintiff's cause of action for patent infringement arises directly from Sharp Corporation's activities in this District.

11. Venue is proper in this Court according to the venue provisions set forth by 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Sharp is subject to personal jurisdiction in this District, and therefore is deemed to reside in this District for purposes of venue. Upon information and belief Sharp has committed acts within this judicial District giving rise to this action and does business in this District, including but not limited to making sales in this District, providing service and support to their respective customers in this District, and/or operating an interactive website, available to persons in this District that advertises, markets, and/or offers for sale infringing products.

BACKGROUND

A. The Patents-In-Suit.

12. U.S. Patent No. 6,359,654 titled "Methods and Systems for Displaying Interlaced Video on Non-Interlaced Monitors" ("the '654 patent") was duly and legally issued by the U.S. Patent and Trademark Office on March 19, 2002, after full and fair examination. Stephen G. Glennon, David A. G. Wilson, Michael J. Brunolli, and Benjamin Edwin Felts, III are the named

inventors listed on the ’654 patent. The ’654 patent has been assigned to Plaintiff Wi-LAN Inc., and Plaintiff Wi-LAN Inc. holds all rights, title, and interest in the ’654 patent, including the right to collect and receive damages for past, present and future infringements. A true and correct copy of the ’654 patent is attached as **Exhibit A** and made a part hereof.

13. U.S. Patent No. 5,847,774 titled “Video Signal Peaking Circuit” (“the ’774 patent”) was duly and legally issued by the U.S. Patent and Trademark Office on December 8, 1998, after full and fair examination. Hyun-Duk Cho is the sole inventor listed on the ’774 patent. The ’774 patent has been assigned to Plaintiff Wi-LAN Inc., and Plaintiff Wi-LAN, Inc. holds all rights, title, and interest in the ’774 patent, including the right to collect and receive damages for past, present and future infringements. A true and correct copy of the ’774 patent is attached as **Exhibit B** and made a part hereof.

14. U.S. Patent No. 6,490,250 titled “Elementary Stream Multiplexer” (“the ’250 patent”) was duly and legally issued by the U.S. Patent and Trademark Office on December 3, 2002, after full and fair examination. Richard Hinchley, Govind Kizhepat and Phillip Love are listed as the inventors on the ’250 patent. The ’250 patent has been assigned to Plaintiff Wi-LAN Inc., and Plaintiff Wi-LAN, Inc. holds all rights, title, and interest in the ’250 patent, including the right to collect and receive damages for past, present and future infringements. A true and correct copy of the ’250 patent is attached as **Exhibit C** and made a part hereof.

15. By assignment, Wi-LAN Inc. owns all right, title, and interest in and to the ’654 patent, the ’774 patent, and ‘250 patents (collectively, “the Patents-in-Suit”).

B. Sharp’s Infringing Conduct.

16. Upon information and belief, Sharp makes, uses, offers to sell, and/or sells within, and/or imports into the United States display products that incorporate the fundamental technologies covered by the Patents-in-Suit. Upon information and belief, the infringing display

products include, but are not limited to, digital televisions. By way of example only, Plaintiff identifies the LC-40LE830U, LC-60LE650U, LC-60LE847U, and LC-60LE857U digital televisions as infringing products of one or more of the Patents-in-Suit. Similar models of Sharp digital televisions are believed to infringe as well.

17. By incorporating the fundamental inventions covered by the Patents-in-Suit, Sharp can make improved products with features, including but not limited to, accurate display of interlaced video on a non-interlaced display, enhanced transitions in displayed images, and adjusting rates of streaming media data. Upon information and belief, third-party distributors purchase and have purchased Sharp's infringing display products for sale or importation into the United States, including this District. Upon information and belief, third-party consumers use and have used Sharp's infringing display products in the United States, including this District.

18. Upon information and belief, Sharp has purchased infringing display products that are made, used, offered for sale, sold within, and/or imported into the United States, including this District by third party manufacturers, distributors, and/or importers.

COUNT I

Patent Infringement of U.S. Patent No. 6,359,654

19. Plaintiff repeats and re-alleges each and every allegation of paragraphs 1-18 as though fully set forth herein.

20. The '654 patent is valid and enforceable.

21. Sharp has never been licensed, either expressly or impliedly, under the '654 patent.

22. Upon information and belief, to the extent any marking or notice was required by 35 U.S.C. § 287, Plaintiff has complied with the requirements of that statute by providing actual or constructive notice to Sharp of its alleged infringement. Upon information and belief, Plaintiff

surmises that any express licensees of the ’654 patent have complied with the marking requirements of 35 U.S.C. § 287 by placing a notice of the ’654 patent on all goods made, offered for sale, sold within, and/or imported into the United States that embody one or more claims of that patent.

23. Upon information and belief, Sharp has been and is directly infringing under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, and/or indirectly infringing, by way of inducement with specific intent under 35 U.S.C. § 271(b), the ’654 patent by making, using, offering to sell, and/or selling to third-party manufacturers, distributors, and/or consumers (directly or through intermediaries and/or subsidiaries) in this District and elsewhere within the United States and/or importing into the United States, without authority, display products that include all of the limitations of one or more claims of the ’654 patent, including but not limited to digital televisions (*e.g.*, the LC-40LE830U, and LC-60LE847U), their display components, and/or other products made, used, sold, offered for sale, or imported by Sharp that include all of the limitations of one or more claims of the ’654 patent.

24. Upon information and belief, distributors and consumers that purchase Sharp’s products that include all of the limitations of one or more claims of the ‘654 patent, including but not limited to digital televisions (*e.g.*, the LC-40LE830U, and LC-60LE847U), also directly infringe, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a), the ’654 patent by using, offering to sell, and/or selling infringing display products in this District and elsewhere in the United States.

25. Upon information and belief, the third-party manufacturers, distributors, and importers that sell display products to Sharp that include all of the limitations of one or more claims of the ’654 patent, also directly infringe, either literally or under the doctrine of

equivalents, under 35 U.S.C. § 271(a), the ’654 patent by making, offering to sell, and/or selling infringing products in this District and elsewhere within the United States and/or importing infringing products into the United States.

26. Upon information and belief, Sharp had knowledge of the ’654 patent and its infringing conduct at least since April 3, 2013, when Sharp was formally placed on notice of its infringement.

27. Upon information and belief, since at least the above-mentioned date when Plaintiff formally placed Sharp on notice of its infringement, Sharp has actively induced, under U.S.C. § 271(b), third-party manufacturers, distributors, importers and/or consumers to directly infringe one or more claims of the ’654 patent. Since at least the notice provided on the above-mentioned date, Sharp does so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the ’654 patent. Upon information and belief, Sharp intends to cause infringement by these third-party manufacturers, distributors, importers, and/or consumers. Sharp has taken affirmative steps to induce their infringement by, *inter alia*, creating advertisements that promote the infringing use of display products, creating established distribution channels for these products into and within the United States, purchasing these products, manufacturing these products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States.

28. Upon information and belief, Sharp’s acts of infringement of the ’654 patent have been willful and intentional. Since at least the above-mentioned date of notice, Sharp has acted with an objectively high likelihood that its actions constituted infringement of the ’654 patent by

refusing to take a license and continuing to make and sell its display products, including but not limited to digital televisions (*e.g.*, the LC-40LE830U, and LC-60LE847U), and the objectively-defined risk was either known or so obvious that it should have been known.

29. As a direct and proximate result of these acts of patent infringement, Sharp has encroached on the exclusive rights of Plaintiff and its licensees to practice the '654 patent, for which Plaintiff is entitled to at least a reasonable royalty.

COUNT II

Patent Infringement of U.S. Patent No. 5,847,774

30. Plaintiff repeats and re-alleges each and every allegation of paragraphs 1-29 as though fully set forth herein.

31. The '774 patent is valid and enforceable.

32. Sharp has never been licensed, either expressly or impliedly, under the '774 patent.

33. Upon information and belief, to the extent any marking or notice was required by 35 U.S.C. § 287, Plaintiff has complied with the requirements of that statute by providing actual or constructive notice to Sharp of its alleged infringement. Upon information and belief, Plaintiff surmises that any express licensees of the '774 patent have complied with the marking requirements of 35 U.S.C. § 287 by placing a notice of the '774 patent on all goods made, offered for sale, sold within, and/or imported into the United States that embody one or more claims of that patent.

34. Upon information and belief, Sharp has been and is directly infringing under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, and/or indirectly infringing, by way of inducement with specific intent under 35 U.S.C. § 271(b), the '774 patent by making, using, offering to sell, and/or selling to third-party manufacturers, distributors, and/or consumers

(directly or through intermediaries and/or subsidiaries) in this District and elsewhere within the United States and/or importing into the United States, without authority, display products that include all of the limitations of one or more claims of the ’774 patent, including but not limited to digital televisions (*e.g.*, the LC-60LE650U and LC-60LE847U), their display components, and/or other products made, used, sold, offered for sale, or imported by Sharp that include all of the limitations of one or more claims of the ’774 patent.

35. Upon information and belief, distributors and consumers that purchase Sharp’s products that include all of the limitations of one or more claims of the ’774 patent, including but not limited to digital televisions (*e.g.*, the LC-60LE650U and LC-60LE847U), also directly infringe, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a), the ’774 patent by using, offering to sell, and/or selling infringing display products in this District and elsewhere in the United States.

36. Upon information and belief, the third-party manufacturers, distributors, and importers that sell display products to Sharp that include all of the limitations of one or more claims of the ’774 patent, also directly infringe, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a), the ’774 patent by making, offering to sell, and/or selling infringing products in this District and elsewhere within the United States and/or importing infringing products into the United States.

37. Upon information and belief, Sharp had knowledge of the ’774 patent and its infringing conduct at least since August 21, 2013, when Sharp was formally placed on notice of its infringement.

38. Upon information and belief, since at least the above-mentioned date when Plaintiff formally placed Sharp on notice of its infringement, Sharp has actively induced, under

U.S.C. § 271(b), third-party manufacturers, distributors, importers and/or consumers to directly infringe one or more claims of the ’774 patent. Since at least the notice provided on the above-mentioned date, Sharp does so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the ’774 patent. Upon information and belief, Sharp intends to cause infringement by these third-party manufacturers, distributors, importers, and/or consumers. Sharp has taken affirmative steps to induce their infringement by, *inter alia*, creating advertisements that promote the infringing use of display products, creating established distribution channels for these products into and within the United States, purchasing these products, manufacturing these products in conformity with U.S. laws and regulations, distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States.

39. Upon information and belief, Sharp’s acts of infringement of the ’774 patent have been willful and intentional. Since at least the above-mentioned date of notice, Sharp has acted with an objectively high likelihood that its actions constituted infringement of the ’774 patent by refusing to take a license and continuing to make and sell its display products, including but not limited to digital televisions (*e.g.*, the LC-60LE650U and LC-60LE847U), and the objectively-defined risk was either known or so obvious that it should have been known.

40. As a direct and proximate result of these acts of patent infringement, Sharp has encroached on the exclusive rights of Plaintiff and its licensees to practice the ’774 patent, for which Plaintiff is entitled to at least a reasonable royalty.

COUNT III

Patent Infringement of U.S. Patent No. 6,490,250

41. Plaintiff repeats and re-alleges each and every allegation of paragraphs 1-40 as though fully set forth herein.

42. The ’250 patent is valid and enforceable.

43. Sharp has never been licensed, either expressly or impliedly, under the ’250 patent.

44. Upon information and belief, to the extent any marking or notice was required by 35 U.S.C. § 287, Plaintiff has complied with the requirements of that statute by providing actual or constructive notice to Sharp of its alleged infringement. Upon information and belief, Plaintiff surmises that any express licensees of the ’250 patent have complied with the marking requirements of 35 U.S.C. § 287 by placing a notice of the ’250 patent on all goods made, offered for sale, sold within, and/or imported into the United States that embody one or more claims of that patent.

45. Upon information and belief, Sharp has been and is directly infringing under 35 U.S.C. § 271(a), either literally or under the doctrine of equivalents, and/or indirectly infringing, by way of inducement with specific intent under 35 U.S.C. § 271(b), the ’250 patent by making, using, offering to sell, and/or selling to third-party manufacturers, distributors, and/or consumers (directly or through intermediaries and/or subsidiaries) in this District and elsewhere within the United States and/or importing into the United States, without authority, display products that include all of the limitations of one or more claims of the ’250 patent, including but not limited to digital televisions (*e.g.*, the LC-60LE650U and LC-60LE857U), their display components, and/or other products made, used, sold, offered for sale, or imported by Sharp that include all of the limitations of one or more claims of the ’250 patent.

46. Upon information and belief, distributors and consumers that purchase Sharp's products that include all of the limitations of one or more claims of the '250 patent, including but not limited to digital televisions (*e.g.*, the LC-60LE650U and LC-60LE857U), also directly infringe, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a), the '250 patent by using, offering to sell, and/or selling infringing display products in this District and elsewhere in the United States.

47. Upon information and belief, the third-party manufacturers, distributors, and importers that sell display products to Sharp that include all of the limitations of one or more claims of the '250 patent, also directly infringe, either literally or under the doctrine of equivalents, under 35 U.S.C. § 271(a), the '250 patent by making, offering to sell, and/or selling infringing products in this District and elsewhere within the United States and/or importing infringing products into the United States.

48. Upon information and belief, since at least the above-mentioned date when Plaintiff formally placed Sharp on notice of its infringement, Sharp has actively induced, under U.S.C. § 271(b), third-party manufacturers, distributors, importers and/or consumers to directly infringe one or more claims of the '250 patent. Since at least the notice provided on the above-mentioned date, Sharp does so with knowledge, or with willful blindness of the fact, that the induced acts constitute infringement of the '250 patent. Upon information and belief, Sharp intends to cause infringement by these third-party manufacturers, distributors, importers, and/or consumers. Sharp has taken affirmative steps to induce their infringement by, *inter alia*, creating advertisements that promote the infringing use of display products, creating established distribution channels for these products into and within the United States, purchasing these products, manufacturing these products in conformity with U.S. laws and regulations,

distributing or making available instructions or manuals for these products to purchasers and prospective buyers, and/or providing technical support, replacement parts, or services for these products to these purchasers in the United States.

49. Upon information and belief, Sharp's acts of infringement of the '250 patent have been willful and intentional. Since at least the above-mentioned date of notice, Sharp has acted with an objectively high likelihood that its actions constituted infringement of the '250 patent by refusing to take a license and continuing to make and sell its display products, including but not limited to digital televisions (*e.g.*, the LC-60LE650U and LC-60LE857U), and the objectively-defined risk was either known or so obvious that it should have been known.

50. As a direct and proximate result of these acts of patent infringement, Sharp has encroached on the exclusive rights of Plaintiff and its licensees to practice the '250 patent, for which Plaintiff is entitled to at least a reasonable royalty.

CONCLUSION

51. Plaintiff is entitled to recover from Sharp the damages sustained by Plaintiff as a result of Sharp's wrongful acts in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

52. Plaintiff has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute create an exceptional case within the meaning of 35 U.S.C. § 285, and Plaintiff is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

53. Plaintiff hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

54. Plaintiff respectfully requests that the Court find in its favor and against Sharp, and that the Court grants Plaintiff the following relief:

A. A judgment that Sharp has infringed the Patents-in-Suit as alleged herein, directly and/or indirectly by way of inducing infringement of such patents;

B. A judgment for an accounting of all damages sustained by Plaintiff as a result of the acts of infringement by Sharp;

C. A judgment and order requiring Sharp to pay Plaintiff damages under 35 U.S.C. § 284, including up to treble damages for willful infringement as provided by 35 U.S.C. § 284, and any royalties determined to be appropriate;

D. A permanent injunction enjoining Sharp and its officers, directors, agents, servants, employees, affiliates, divisions, branches, subsidiaries, parents and all others acting in concert or privity with them from direct and/or indirect infringement of the Patents-in-Suit pursuant to 35 U.S.C. § 283;

E. A judgment and order requiring Sharp to pay Plaintiff pre-judgment and post-judgment interest on the damages awarded;

F. A judgment and order finding this to be an exceptional case and requiring Sharp to pay the costs of this action (including all disbursements) and attorneys' fees as provided by 35 U.S.C. § 285; and

G. Such other and further relief as the Court deems just and equitable.

Dated: May 11, 2015

Respectfully submitted,

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EXHIBIT A

US006359654B1

(12) **United States Patent**
Glennon et al.

(10) **Patent No.: US 6,359,654 B1**
(45) **Date of Patent: Mar. 19, 2002**

(54) **METHODS AND SYSTEMS FOR DISPLAYING INTERLACED VIDEO ON NON-INTERLACED MONITORS**

(75) Inventors: **Stephen G. Glennon**, Cedar Park; **David A. G. Wilson**, Austin, both of TX (US); **Michael J. Brunolli**, Escondido; **Benjamin Edwin Felts, III**, Cardiff, both of CA (US)

(73) Assignee: **Conexant Systems, Inc.**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/798,240**

(22) Filed: **Feb. 12, 1997**

Related U.S. Application Data

(60) Provisional application No. 60/011,656, filed on Feb. 14, 1996.

(51) **Int. Cl.**[7] **H04N 7/01**; H04N 11/20

(52) **U.S. Cl.** **348/448**; 348/458; 348/440

(58) **Field of Search** 348/448, 449, 348/454, 455, 456, 458, 459, 446, 445, 443, 441, 558, 556, 555, 543, 544, 545, 546, 576; H07N 7/01, 11/20, 7/20

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WO	WO 94/15435	7/1994	H04N/7/01

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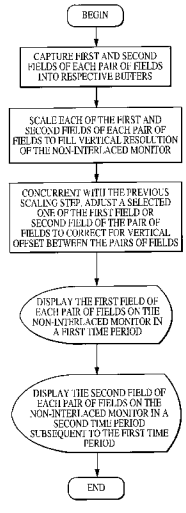
Primary Examiner—Andrew Faile
Assistant Examiner—Vivek Srivastava
(74) *Attorney, Agent, or Firm*—Jaquez & Associates; Martin J. Jaquez, Esq.

(57) **ABSTRACT**

A number of methods to display interlaced video on non-interlaced monitor are disclosed. One method is to display all of the incoming fields but one at a time, and correcting for the positional offset of one field relative to another in the interlaced data. An important aspect of the present invention is the correction of the positional offset of the two interlaced video fields. There are two ways presented to deal with the vertical offset of the two fields in accordance with the present invention. The first way is that the two fields can be displayed at different positions on the display using a non-interlaced display. The second way is that the video data can be altered to correct the positional offset between the fields. Another method of the present invention is to lock the frame rate of the output video to the incoming field rate or a multiple of the incoming field rate, or to certain sub-multiples of the incoming field rate. An important feature of this method is that each frame of the output monitor need not match the incoming field time precisely. As long as each output frame is displayed exactly the predetermined number of times, the appearance of smooth motion will be maintained.

18 Claims, 6 Drawing Sheets



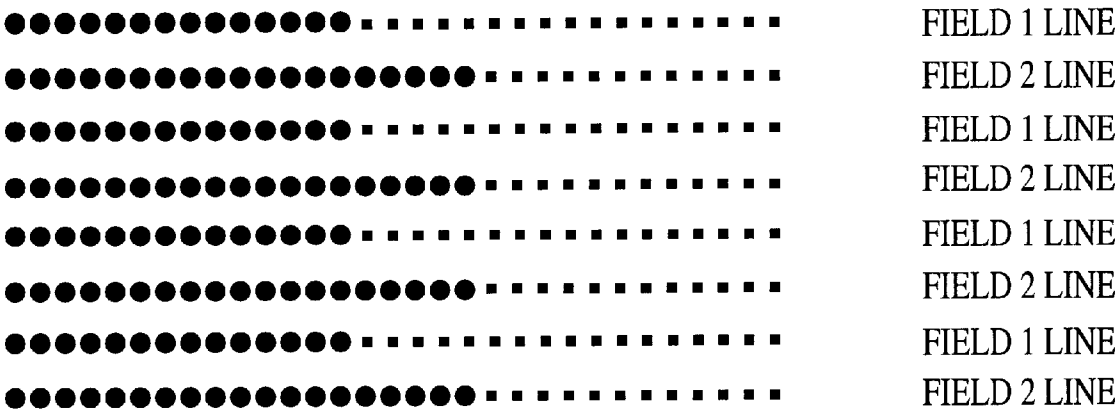


FIGURE 1
(PRIOR ART)

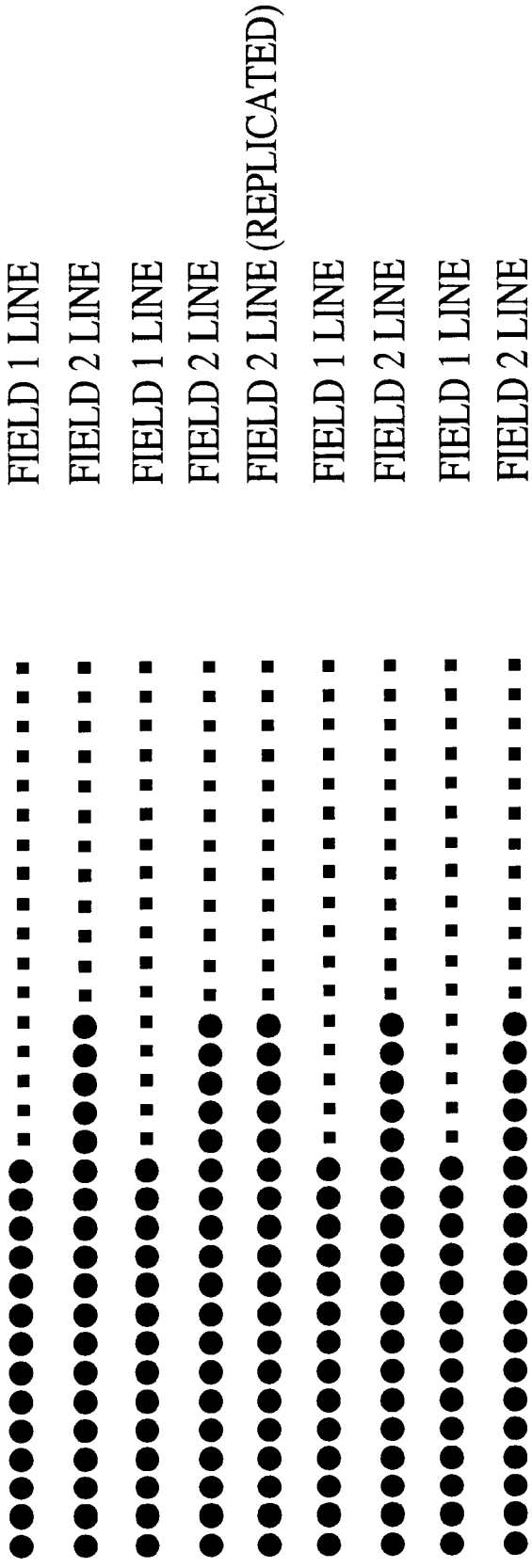


FIGURE 2
(PRIOR ART)

A NTSC FIELD	B FILM FRAME USED	C TOTAL TIME FRAME TRANSMITTED (ms)	D IMAGE CAPTURED	E TOTAL TIME IMAGE DISPLAYED (ms)
1 (ODD)	1	50	1	66.6
2 (EVEN)	1			
3 (ODD)	1		1	
4 (EVEN)	2	33.3		
5 (ODD)	2		2	33.3
6 (EVEN)	3	50		
7 (ODD)	3		3	33.3
8 (EVEN)	3			
9 (ODD)	4	33.3	4	33.3
10 (EVEN)	4			
11 (ODD)	5	50	5	66.6
12 (EVEN)	5			
13 (ODD)	5		5	
14 (EVEN)	6	33.3		
15 (ODD)	6		6	33.3
16 (EVEN)	7	50		
17 (ODD)	7		7	33.3
18 (EVEN)	7			
19 (ODD)	8	33.3	8	33.3
20 (EVEN)	8			
21 (ODD)	9	50	9	66.6
22 (EVEN)	9			
23 (ODD)	9		9	
24 (ODD)	10	33.3		
25 (EVEN)	10		10	33.3
26 (ODD)	11	50		
27 (EVEN)	11		11	33.3
28 (ODD)	11			

FIGURE 3
(PRIOR ART)

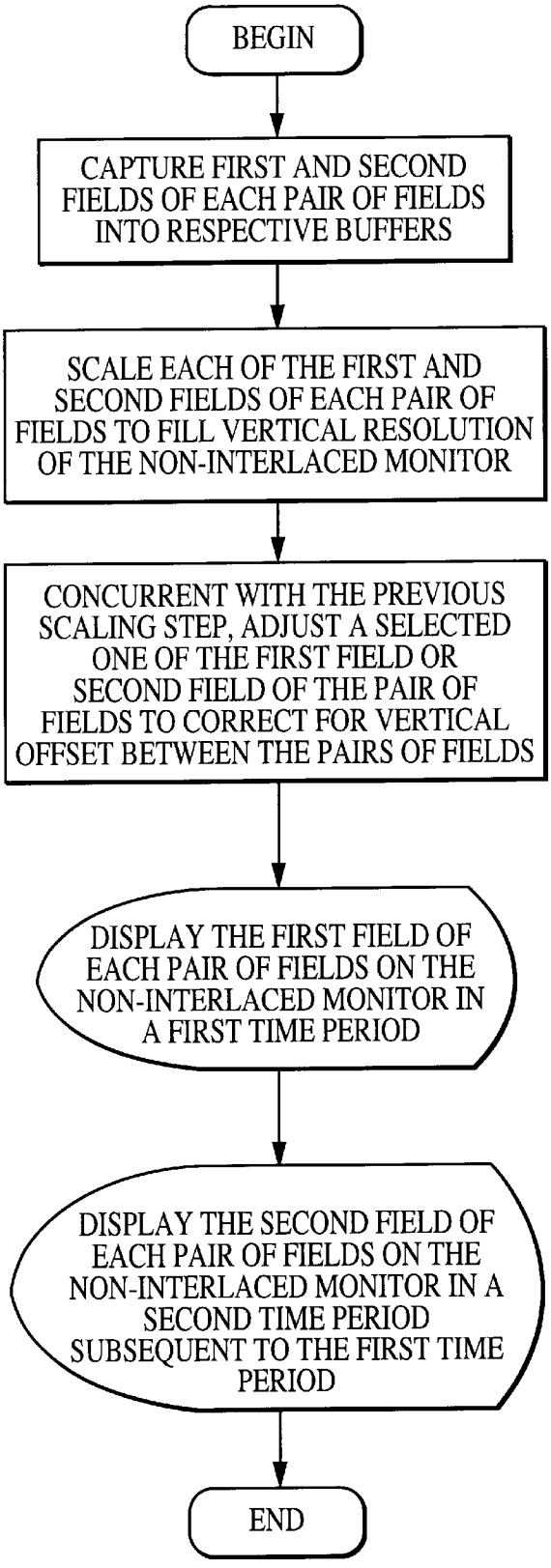

BEGIN
CAPTURE FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS INTO RESPECTIVE BUFFERS
SCALE EACH OF THE FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS TO FILL VERTICAL RESOLUTION OF THE NON-INTERLACED MONITOR
CONCURRENT WITH THE PREVIOUS SCALING STEP, ADJUST A SELECTED ONE OF THE FIRST FIELD OR SECOND FIELD OF THE PAIR OF FIELDS TO CORRECT FOR VERTICAL OFFSET BETWEEN THE PAIRS OF FIELDS
DISPLAY THE FIRST FIELD OF EACH PAIR OF FIELDS ON THE NON-INTERLACED MONITOR IN A FIRST TIME PERIOD
DISPLAY THE SECOND FIELD OF EACH PAIR OF FIELDS ON THE NON-INTERLACED MONITOR IN A SECOND TIME PERIOD SUBSEQUENT TO THE FIRST TIME PERIOD
END

FIGURE 4

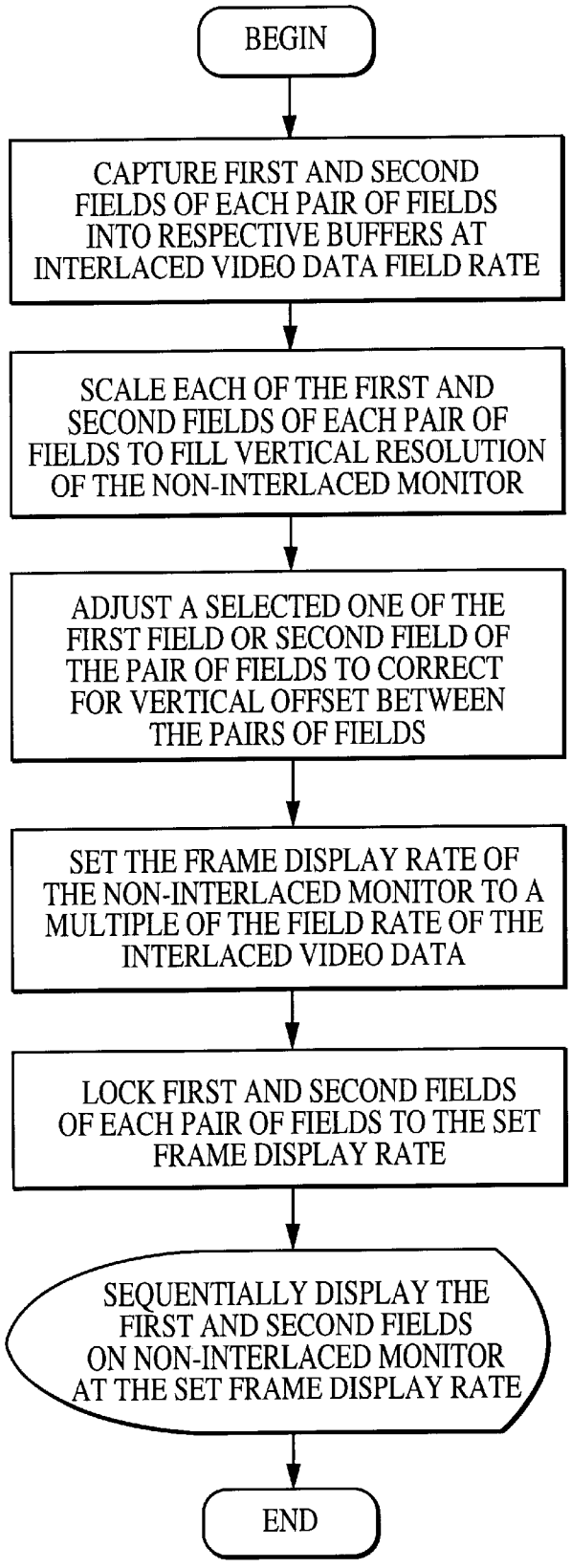

BEGIN
CAPTURE FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS INTO RESPECTIVE BUFFERS AT INTERLACED VIDEO DATA FIELD RATE
SCALE EACH OF THE FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS TO FILL VERTICAL RESOLUTION OF THE NON-INTERLACED MONITOR
ADJUST A SELECTED ONE OF THE FIRST FIELD OR SECOND FIELD OF THE PAIR OF FIELDS TO CORRECT FOR VERTICAL OFFSET BETWEEN THE PAIRS OF FIELDS
SET THE FRAME DISPLAY RATE OF THE NON-INTERLACED MONITOR TO A MULTIPLE OF THE FIELD RATE OF THE INTERLACED VIDEO DATA
LOCK FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS TO THE SET FRAME DISPLAY RATE
SEQUENTIALLY DISPLAY THE FIRST AND SECOND FIELDS ON NON-INTERLACED MONITOR AT THE SET FRAME DISPLAY RATE
END

FIGURE 5

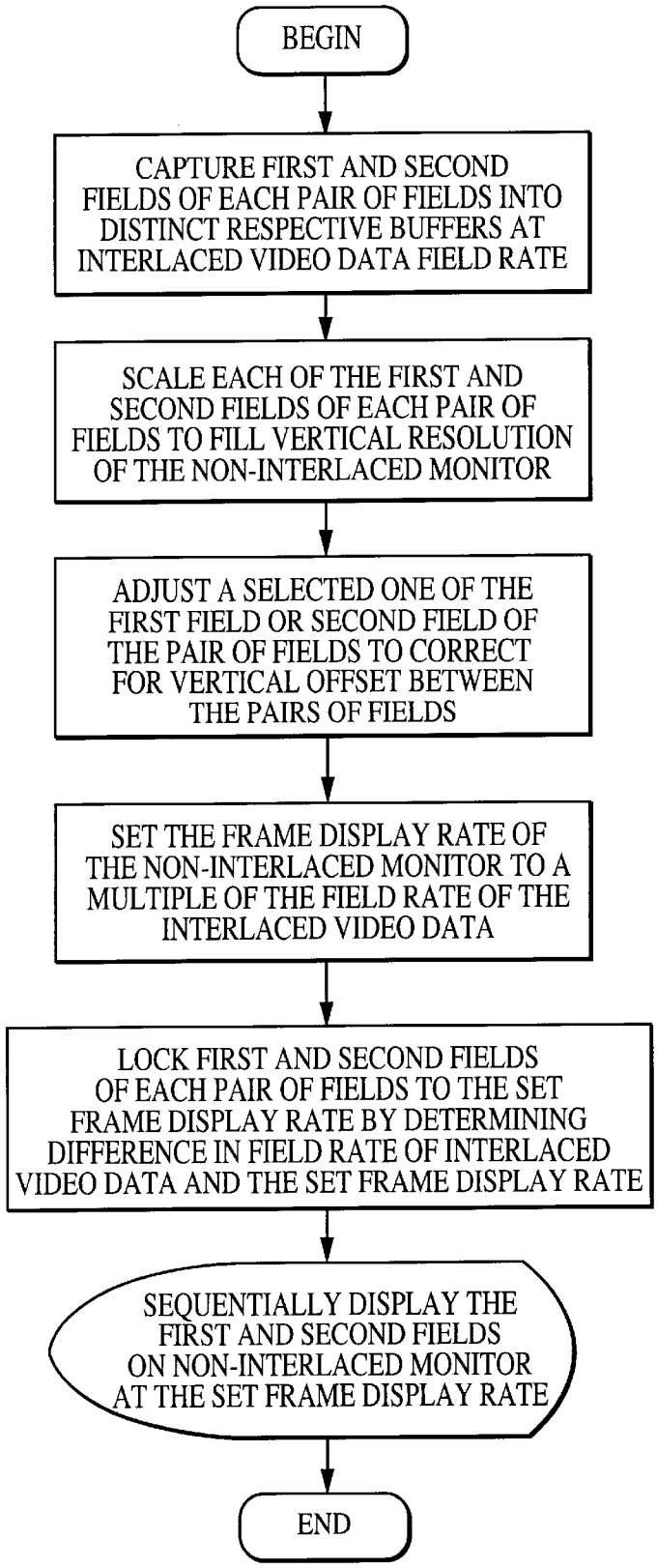

BEGIN
CAPTURE FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS INTO DISTINCT RESPECTIVE BUFFERS AT INTERLACED VIDEO DATA FIELD RATE
SCALE EACH OF THE FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS TO FILL VERTICAL RESOLUTION OF THE NON-INTERLACED MONITOR
ADJUST A SELECTED ONE OF THE FIRST FIELD OR SECOND FIELD OF THE PAIR OF FIELDS TO CORRECT FOR VERTICAL OFFSET BETWEEN THE PAIRS OF FIELDS
SET THE FRAME DISPLAY RATE OF THE NON-INTERLACED MONITOR TO A MULTIPLE OF THE FIELD RATE OF THE INTERLACED VIDEO DATA
LOCK FIRST AND SECOND FIELDS OF EACH PAIR OF FIELDS TO THE SET FRAME DISPLAY RATE BY DETERMINING DIFFERENCE IN FIELD RATE OF INTERLACED VIDEO DATA AND THE SET FRAME DISPLAY RATE
SEQUENTIALLY DISPLAY THE FIRST AND SECOND FIELDS ON NON-INTERLACED MONITOR AT THE SET FRAME DISPLAY RATE
END

FIGURE 6

METHODS AND SYSTEMS FOR DISPLAYING INTERLACED VIDEO ON NON-INTERLACED MONITORS

CROSS-REFERENCE TO RELATED PROVISIONAL APPLICATION

This application claims the benefit of U.S. Provisional Application, Ser. No. 60/011,656, filed on Feb. 14, 1996.

FIELD OF THE INVENTION

The present invention relates to computer display systems, and particularly to methods and systems for displaying interlaced video on monitors which are non-interlaced.

BACKGROUND OF THE INVENTION

Until now there have been two commonly used simple methods for displaying interlaced video being fed into the computer system on a computer monitor. These are normally independent of whether the computer monitor is interlaced or not, as even when the monitor is interlaced it normally refreshes at a rate independent of the incoming video signal.

Throughout this description NTSC video is assumed for the sake of illustrative examples, with references to 240 line fields, 480 line frames, 60 fields per second and 30 frames per second. This does not restrict the invention to NTSC or the line counts or frame or field rates but is merely used for simplicity. The invention is equally applicable to other video standards such as, but not limited to, PAL with 288 line fields, 576 line frames, 50 fields per second and 25 frames per second.

The first method is just capturing one of the two fields, and displaying 240 lines scaled (interpolated) up to 480 or however many are in the current display mode. The special case of scaling to 480 lines (line doubling) is currently used in the art and is well documented. See pages 332–333 of "Video Demystified: a Handbook for the Digital Engineers" by Keith Jack, HighText Publication Inc., 1993 (referred to herein as "Keith Jack").

The second method is to perform simple de-interlacing where both fields are captured into a single 480 line buffer and double the buffer line length for a single field in order to store a field in every other line. This is referred to as "Field Merging" (see p. 333 of Keith Jack)

(1) Deinterlacing by interleaving two fields into a single buffer

This method is fine in theory and provides better vertical resolution than a single field 240 line capture, but gives very objectionable results when viewing video with rapid horizontal action (for example a football game), as noted in page 333 of Keith Jack.

As the two fields of a single video image are separated in time by 1/60th of a second, storing the later field interweaved into the same buffer results in a image with a zipper like appearance along high contrast vertical edges when rapid horizontal motion takes place in the source video. This effect is illustrated in FIG. **1** of the present application. Page 335, FIG. 7 of Keith Jack uses a picture of a flying bird to illustrate this artefact.

Another problem to compound these line to line zipper like artefacts occurs when one needs to scale the resulting 480 line video up to different sizes. When one scales up by line replication, at certain points in the vertical scaling it is necessary to display one of the lines twice. If the image already has a repetitive left-right-left-right-left-right offset on vertical edges, replicating a single line introduces what appears as another break in the video. The effect can be seen in FIG. **2**.

These breaks appear in a regular pattern, dictated by the scaling factor used to scale up from 480 lines to the destination size (for example 600 or 768 lines).

Pages 333–336 of Keith Jack refer to advanced techniques requiring detection of motion between fields on a pixel by pixel basis requiring the storage of 4 fields. This processing on a pixel by pixel basis would typically be expensive to implement because of the requirement for storing 4 fields and attempting to compare and process pixels from two fields to generate each output pixel.

Vertical interpolation can help to reduce this second artefact by attempting to interpolate between the lines from the two fields, but still does not give visually pleasing results.

(2) Displaying a single field per frame

Displaying a single field from a frame has an advantage, but some definite problems. The advantage is that there are none of the artefacts described above relating to the interleaving of two time-separated fields into a single buffer. There are three main problems. The first problem is that the image generated is fundamentally lower resolution vertically, coming from only 240 lines. Keith Jack refers to this when discussing "Scan Line Duplication" and "Scan Line Interpolation," indicating that although the number of lines is doubled, the vertical resolution is not increased from the original data (see pages 332–333 of Keith Jack). In addition, Keith Jack only deals with displaying on a 480 line display where the number of lines is exactly doubled. Further, Keith Jack only considers displaying a single field because it does not consider the differing spatial aspects of odd and even fields in an interlaced video source.

The second problem is that the image only changes 30 times per second, whereas the source interlaced data changes 60 times per second. Thirty frames per second is often considered "full motion video," indicating that it is good enough to fool the human eye into perceiving smooth motion. However, performing a side by side comparison of 30 and 60 frame per second video makes it apparent that 60 frames per second is noticeably smoother.

The third problem is that displaying a single field at a rate of 30 fields per second interferes with 3:2 pull down commonly used to transmit films shot at 24 frames per second on an NTSC signal at 60 fields per second. With 3:2 pull down, a single film frame is transmitted for either two or three NTSC fields in order to approximate to the nominal 30 frames per second of NTSC. FIG. **3** shows the relationship of the film, the transmitted NTSC fields, and the images displayed on the computer screen.

It can be seen from column C of FIG. **3** that on a conventional TV the successive frames are displayed for 50 ms, 33.3 ms, 50 ms, 33.3 ms, 50 ms, and so on. This rapid alternation between two display times which differ by a factor of 1.5 gives a good impression of smooth motion on a conventional TV.

From column E of FIG. **3**, it can be seen that using and displaying a single field results in the successive frames being displayed for 66.6, 33.3, 33.3, 33.3, 66.6 ms, and so on. Note that the period of the alternation between the short display time and the long display time is two times that of column C, and that the two display times differ by a factor of 2.

Summarizing, column E has a higher variability in the display time and a longer period in the variability. These two

factors result in a noticeable jerkiness in the displayed images, particularly in smooth but rapid horizontal pans in the source film.

Note that in this simplistic analysis the effect of running the video monitor attached to the computer at a rate other than 60 Hz has been ignored. If the monitor is being refreshed at another frequency, (for example the commonly used 75 Hz), the artefacts introduced vary somewhat but the displayed images still show a fundamental jerkiness.

Pages 358–361 of Keith Jack address issues regarding field and frame rate conversion, but only for conversion from a computer monitor non-interlaced to TV interlaced, or from one interlaced standard to another. Keith Jack does not address frame rate conversion from interlaced (e.g., TV) to non-interlaced (e.g., computer monitor) systems. In addition, it refers to the "3:2 pull down" technique illustrated above in columns A and B (see its section on Field and Frame Rate Conversion of page 361 and FIG. 9.36 of page 365) for conversion from 24 frames per second film to 60 fields per second NTSC.

SUMMARY OF THE INVENTION

The following inventions describe ways of displaying interlaced video from sources such as MPEG 1, MPEG 2, Broadcast TV, Cable TV, Satellite TV, Direct Broadcast Satellite (PBS), Direct Satellite System (DSS), Video Tape Recorders (VTR's), LaserDisc, and any other sources of interlaced video, along with non-interlaced MPEG 1 video, on computer systems.

One method used in the present invention is to display all of the incoming fields but one at a time, and correcting for the positional offset of one field relative to another in the interlaced data. The method of doing this is to capture the two fields into separate buffers, one for the odd field and one for the even field. When one of the fields has been captured into the buffer, the buffer is displayed, scaled to the requested dimensions on the monitor using some scaling hardware or software. That image is displayed until the next field is captured into another buffer, and then the subsequent image is displayed until the third field is captured into either the original first buffer, or into another (third) buffer.

An important aspect of the present invention is the correction of the positional offset of the two interlaced video fields. There are two ways presented to deal with the vertical offset of the two fields in accordance with the present invention. The first way is that the two fields can be displayed at different positions on the display using a non-interlaced display. The second way is that the video data can be altered to correct the positional offset between the fields.

Another method of the present invention is to lock the frame rate of the output video to the incoming field rate or a multiple of the incoming field rate, or to certain sub-multiples of the incoming field rate. This is a much looser coupling of rates than conventional genlocking, and consequently can be implemented much more cheaply. All that is required to ensure that each field is displayed for the predetermined number of frame times on the output monitor. If the output frame rate is being made the same as the incoming field rate, then each field needs to be shown exactly once. This results in a frame rate of the output display of exactly the incoming field rate (59.94 hertz for NTSC, 50.00 hertz for PAL and SECAM). Similarly, for an output monitor rate of twice the incoming field rate, each field is displayed for exactly two output frames.

An important feature of this method is that each frame of the output monitor need not match the incoming field time precisely. As long as each output frame is displayed exactly the predetermined number of times, the appearance of smooth motion will be maintained.

These and other features of the present invention will become apparent from the following description when read in conjunction with the drawings and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a prior art method of deinterlacing by interleaving two fields into a single buffer.

FIG. **2** shows another prior art method of deinterlacing by interleaving two fields into a single buffer.

FIG. **3** shows a prior art method of displaying a single field per frame.

FIG. **4** is a flowchart of one embodiment of the present inventive method for displaying interlaced video data on a non-interlaced monitor.

FIG. **5** is a flowchart of another embodiment of the present inventive method for displaying interlaced video data on a non-interlaced monitor.

FIG. **6** is a flowchart of yet another embodiment of the present inventive method for displaying interlaced video data on a non-interlaced monitor.

DETAILED DESCRIPTION OF THE INVENTION

The present invention comprises a novel graphic display system and related methods. The following description is presented to enable any person skilled in the art to make and use the invention. Description of specific applications are provided only as examples. Various modifications to the preferred embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

(1) Display All Fields

One feature of the present invention is to display all of the incoming fields but one at a time, and correcting for the positional offset of one field relative to another in the interlaced data. The method of doing this is to capture the two fields into separate buffers, one for the odd field and one for the even field. When one of the fields has been captured into the buffer, the buffer is displayed, scaled to the requested dimensions on the monitor using some scaling hardware or software. Typically, scaling can be achieved using line replication, line dropping, or a filtered scaling method such as interpolation.

That image is displayed until the next field is captured into another buffer, and then the subsequent image is displayed until the third field is captured into either the original first buffer, or into another (third) buffer.

The multiple buffering is to ensure that a video buffer is not being updated while it is being displayed, to avoid "tearing" (a horizontal discontinuity in the displayed data caused by the simultaneous display of part of one field and part of the following field)—a technique commonly known in the art and discussed in Keith Jack (see pages 358–359).

This method works well for MPEG 1 data which is 60 field per second, but is not actually interlaced, as each field being output by the MPEG 1 decoder is from the same vertical offset in the source image. However, for truly

interlaced video odd fields and even fields are not from exactly the same place in the image. For truly interlaced video the odd and even fields are from positions one half a line different (vertically) in the original image. If the two fields are displayed "as is" in the same position on the output screen, it appears that the image is rapidly jiggling up and down. In order to display the fields in a way which eliminates this artefact, it is necessary to either display the odd and even fields in different positions on the display, or to alter the data before it is displayed to correct this vertical offset between the two fields.

An important aspect of the present invention is the correction of the positional offset of the two interlaced video fields. There are two ways presented to deal with the vertical offset of the two fields in accordance with the present invention.

(a) The two fields can be displayed at different positions on the display using a non-interlaced display.

The video data in each field consists of 240 lines of active data for NTSC video. If this is scaled up to twice that number of lines on the display, changing the position of scaled up image by a single line on the 480 line display effects a half line repositioning of the original 240 line image, correcting the half line offset of the two fields. One field is displayed at a particular line on the display, and the other field is displayed up one line or down one line on the display (whichever is appropriate for the correct repositioning of the other field—this depends on whether the first field is the odd or the even field).

Repositioning in this way gives the exactly correct repositioning when each field is scaled up by exactly a factor of 2. It is also possible to get exact repositioning when the fields are scaled up by a factor of 4 (by moving one of the fields 2 lines on the display), 6 (by moving one of the fields 3 lines on the display), or by any factor which is exactly divisible by 2. In the above example, a 480 line output monitor is considered but the invention is not limited to that monitor size.

It is possible and desirable to perform repositioning for other vertical scale factors, but the repositioning does not exactly correct for the vertical offset of the original fields. The repositioning should be performed whenever the resulting effective offset of the two fields is less than one half a line in the 240 line source data, as this gives visually more pleasing results than when the data is not adjusted, and has a positional error of 0.5 lines.

The above description applies to incoming NTSC field data which has not been scaled, but is not limited to this case. It is applicable to other field sizes (generated by other video standards such as PAL and SECAM), or when the field data is scaled vertically before being stored in the memory buffers. In these other cases, the output sizes would be determined by using the same scale up factors of 2, 4, 6 and so on.

The two fields can be scaled up using techniques including line replication and vertical interpolation. Vertical interpolation gives significantly better visible results than line replication, reducing apparent vertical "blockiness" of the displayed image, and smoothing angled lines in the video data which can have pronounced "stair step" appearance when line replication is used. Vertical interpolation should be used when scaling to factors which are not a multiple of 2, as line replication introduces additional visual artefacts in these cases.

Prior art methods do not consider repositioning alternate fields. As an example, even though Keith Jack discloses using deinterlacing with scan line interpolation, it does not consider the vertical offset of alternate video fields (see FIG. 9.4 on page 333). In addition, Keith Jack only considers producing two output lines for each input line, which would restrict the output monitor to displaying 480 lines for NTSC or 576 lines for PAL (having fields containing 240 active lines and 288 active lines respectively). This is highly undesirable in current situations where computer monitors are typically operated in modes with 600, 768, 1024 or 1200 lines.

(b) The video data can be altered to correct the positional offset between the fields.

It is possible to modify the video data to correct for the positional difference in the fields. In the simplest case, one of the fields can be re-sampled vertically such that the pixels of a displayed line are generated by averaging two vertically adjacent pixels from two lines. The resulting averaged pixel is effectively a pixel positioned half way between the two lines, thereby implementing a half line vertical repositioning.

This approach is very attractive, as it can be implemented for little or no additional cost on hardware which already has a vertical interpolator. All that is required is the ability to set the initial value of the vertical interpolator such that the first line it generates is 50% of the top line and 50% of the line after the top line. If the same vertical interpolator is used for both odd and even fields it is necessary to be able to alter the initial line behavior on a field to field basis, so that one field can be generated with the first line being 100% of the first line of the incoming data (that is, no vertical repositioning), and the other field being generated using 50% line 1 and 50% line 2 for the first stored/displayed line.

Although the description above in connection with the above described second way (i.e., the video data can be altered to correct the positional offset between the fields) has implied use of the vertical repositioning on the input (video capture) side of the hardware, it is applicable to both the input and the output paths. It is possible to perform the interpolative repositioning on the input path, before the video fields are stored in memory, or the video fields can be stored in memory unaltered and the hardware which scales the video on output can affect the interpolative repositioning.

In general, it is more desirable to perform the resampling on the output path for the following reason. If the data is resampled (but not scaled) on the input path, one of the fields will have had each of its lines generated by averaging two lines. This results in a certain amount of smoothing of the picture before the pixels are stored in the frame buffer memory. If this data in the frame buffer is then scale up for display (as is usually the case), then interpolative upscaling on the output path introduces further averaging (of two of the lines in the frame buffer) to generate an output line. This results in further smoothing. The two-pass smoothing can be detrimental to the quality of the output image, making it look much softer (with less detail) than a regular television picture.

If the resampling is performed purely on the output path by manipulating the initial phase of the output interpolator for one of the fields, then the each output line is generated by averaging two input lines a single time, giving a sharper image than the double averaging introduced by resampling on the input path and scaling on the output path.

Performing the resampling and upscaling on the input path is less desirable as the video field must be stored upscaled, thereby using more memory and potentially increasing the cost of the system.

In addition, if the resampling is to be performed on the output path it can be performed using whatever output

resealing scheme is implemented in hardware. This can be (but is not limited to) schemes which vertically scale in the DAC, as the Brooktree BtV 2487 does, or schemes which scale by reading the unscaled data from memory and write it back to memory in the scaled size before the data is displayed. The Brooktree BtV 2487 is a commercially available integrated circuit.

A refinement of this vertical resampling scheme is to resample both fields such that the resulting two fields have the same effective spatial positioning, rather than resample just one of the fields. Performing the vertical resampling has the side effect that it smooths the image slightly. If only one of the fields is resampled then one field has been smoothed and the other has not. This may result in a visible disparity between the two fields when displayed. A scheme where both fields are resampled, but maintain the goal of having the same resulting position would be to resample one of the fields such that the first line output is 25% line one and 75% line two, and the other field is resampled such that the first output line is 75% line one and 25% line two. This still causes a half line repositioning of one output field relative to the other. This approach only adds benefit when the fields are to be shown unscaled (for example as 240 lines for NTSC) on the output monitor. In all other cases of upscaling both fields get smoothed by the upscaling operation (assuming interpolative upscaling) so the potential disparity in the smoothing is eliminated.

As discussed in the preceding paragraph, normal interpolation (averaging) of input lines to generate output lines results in some smoothing of the output image relative to the appearance on a normal television. Interpolation is preferable to line replication as line replication looks "blockier" than normal televisions, but the smoothing also degrades the visual quality slightly. A refinement of the vertical interpolation approach is to generate output lines by using three or more input lines and using a more complex filter which performs regular interpolation for smooth regions (low frequency changes in the vertical picture data), but enhances sharp changes in the picture vertically (high frequency changes in the vertical picture data). This kind of "sharpness filter" can be adjusted to provide the most visually pleasing result for the end viewer.

In addition to eliminating the jerkiness problems discussed above for displaying a single field out of each frame, this approach eliminates the problems of line to line "zippering" as described above for displaying both fields interleaved into a single buffer, and it results in video which had an apparently higher vertical resolution than displaying a single field vertically interpolated up to the output size.

(2) Dealing with Temporal Artefacts

Above was described one of the problems of jerkiness of displayed images when displaying only a single field per frame when the incoming video signal comes from film originally shot at 24 frames per second and re-sampled to be transmitted at 60 fields per second.

In the simplistic treatment above, only the capture rate (60 fields per second) was taken into account. However, one must also take the monitor refresh rate into consideration. Normally, computer monitors are operated at refresh rates of between 56 Hz and 85 Hz. Newer monitors ate often capable of refresh rates significantly in excess cf 85 Hz.

When the monitor refresh rate differs from the rate of the incoming video, it is necessary to use multiple buffers to capture and display the video fields, in order to avoid simultaneously updating and displaying a single buffer. If a memory buffer is simultaneously updated with incoming video data and displayed, the resulting displayed video typically has objectionable "tearing" artefacts where what is seen on the computer display is part of an old field for one portion of the display, and part of the new field for the rest of the display. Where there is rapid motion in the incoming video, the transition from the old field to the new shows up as a horizontal discontinuity in the displayed image (a horizontal "tear" in the image). Normally it is sufficient to make use of two buffers, one for the field being displayed on the monitor, and one for the field currently being captured. For reasons beyond the scope of this description it is necessary to use three buffers to avoid horizontal tearing under certain circumstances (such as when the image being displayed on the computer monitor does not fill the entire screen, and is displayed with the top edge being below the top edge of the screen).

Given the above treatment where multiple buffering is used to avoid horizontal tearing, each field of captured data is displayed for a multiple of display frame times (1 or more). This is currently the state of the art in displaying video on non-interlaced monitors. This approach leads to video with less smooth motion than is typically seen on a standard television, as without some guarantee of displaying at a frame rate locked to the field rate of the video, then some fields will be displayed for multiple display frame times, and some for a single frame time. This variability in the time a particular field is displayed for leads to an apparent jerkiness in the displayed video.

This inherent limitation of current implementations is circumvented by the following feature of the invention: Matching the display rate to the incoming video rate.

Genlocking is a technique known in the art for intimately synchronizing two interlaced video signals in order to allow video mixing and editing from multiple video sources. In genlocking, the finest details of the video signals are synchronized; the sync pulses, the pixel clocks and even the chrominance subcarrier clock. This technique is not applicable to a non-interlaced output display, where the video timings are fundamentally different from the incoming interlaced video signal: the lines cannot be synchronized as there are different numbers of lines between the interlaced field and the output monitor, and this precludes pixel clock synchronization. In addition, the RGB non-interlaced display monitors have no concept of a chrominance subcarrier clock.

One aspect of the present invention is to lock the frame rate of the output video to the incoming field rate or a multiple of the incoming field rate, or to certain submultiples of the incoming field rate. This is a much looser coupling of rates than genlocking, and consequently can be implemented much more cheaply. All that is required to ensure that each field is displayed for the predetermined number of frame times on the output monitor. If the output frame rate is being made the same as the incoming field rate, then each field needs to be shown exactly once. This results in a frame rate of the output display of exactly the incoming field rate (59.94 hertz for NTSC, 50.00 hertz for PAL and SECAM). Similarly, for an output monitor rate of twice the incoming field rate, each field is displayed for exactly two output frames.

Displaying at the same frame rate as the incoming field rate works extremely well when the non-interlaced output monitor has the same type of phosphors as a regular television, as the persistence of the phosphors is classed as "medium" and results in a non-flickering image when refreshed 60 times per second. However, most computer monitors are designed and built with "Short persistence" phosphors. This is because they are typically designed to be

refreshed 75 times per second or more. For these monitors, it would seem that moving to twice the incoming field rate would be ideal. However, for NTSC, this would lead to a refresh rate of 119.88 hertz (hereafter simplified to 120 hertz). Most mid-priced computer monitors are not capable of being refreshed at that rate (normally being limited to at most 100 hertz), especially at larger resolutions such as 1024 pixels wide by 768 lines.

For these cases an acceptable compromise is to lock the monitor to 1.5 times the incoming field rate (approximately 90 hertz). In this case, alternate fields are displayed for exactly 1,2,1,2,1,2,1,2 etc. frame times. This rapid variation in the display time of each field can somewhat fool the human eye into seeing smooth motion. It is still a requirement to lock the rates such that the pattern of frame times is exactly maintained. If this is not done, then at some point the pattern may become 1,2,1,1,2,1,2,1 or 1,2,2,1,2,1,2,1,2 which would result in a visible jerk on certain video scenes containing motion.

An important feature of the invention is that each frame of the output monitor need not match the incoming field time precisely. As long as each output frame is displayed exactly the predetermined number of times, the appearance of smooth motion will be maintained. For example, the nominal field time of NTSC is 16.6833 milliseconds. The display frame time should be made to be very close to this time by the nature of this feature of the invention. However, if the output frame time is smaller than this value, then over a period of several frames the position of the output display refresh gun will drift relative to the position of the incoming video signal. As long as the cumulative error in the display time over a number of frames does not exceed the field time of the incoming video signal, each input field will be displayed once only. If the display frame time can be adjusted to longer than the field time for the incoming video signal, then the cumulative error can be corrected over a period of frames. Over time, the error will reduce to zero, and then accumulate as an error in the opposite direction. At this point, the output frame time should once again be adjusted to less than the incoming field time to correct the new cumulative error. As long as the errors are corrected before they accumulate to a whole frame time, each field will be displayed for single output frame.

There are two aspects to implementing this feature. The first aspect is the ability to adjust the monitor timing without causing a visible artefact on the display. The second aspect is the ability to sense the relative positions and drift in the positions of the video capture signal and the display signal.

There are three methods to achieve the first aspect (i.e., being able to adjust the monitor timing without causing a visible artefact on the display):

i) The preferred method for speeding up and slowing down the display is to remove or add pixels to the display lines in the vertically blanked region. The best place to add or remove pixels is as early in the blanking region as possible. This is because display monitors set their line and frame frequency from the incoming signals; if these signals change then the internal phase locked loop circuits in the monitors will lock onto the new frequencies. Making changes to the number of pixels in a line (changing the line frequency) early in the blanking allows the monitor's phase locked loop circuits to lock back to the normal line frequency before the active video is displayed.

ii) It is also possible to add or remove lines from the monitor's refresh, but this often causes vertical instability in the monitor's display when the line is added or removed. This instability is visible to viewer, making this approach less attractive.

iii) It is possible to adjust the frequency of the clock used to generate the output display to slow down or speed up the display. In this case it is important that the granularity of change is extremely fine such that the change does not cause the display to visibly alter in size or position. It is unusual to have sufficiently fine granularity to make this method viable.

Three methods are presented here as examples of ways to achieve the second aspect (i.e., being able to sense the relative positions and drift in the positions of the video capture signal and the display signal):

i) If it is possible to sense the position of one of the signals but not the other, one can determine the relative position of the two signals by sampling the available position at a fixed time in the refresh cycle of the other signal. Typically it is possible to generate a signal at a set time in either the display refresh cycle (most computer graphics systems can generate an interrupt at vertical retrace time) or in the incoming video circuitry (often through a frame complete interrupt). At the time of the interrupt the code samples the available position (often implemented as a line counter) and compares this to a similar value obtained from previous occasions. From this history, the system can determine the rate of drift and the relative positions of the signals and can adjust the output monitor timings to compensate.

ii) If two line counters are available, one for the input circuitry and one for the output circuitry, they can be sampled at the same time, and subtracted to determine a difference in position. Similarly to method (i) above, a history can be maintained and corrections made to the output timing as appropriate.

iii) If the input and output circuits are linked, then it is possible to implement a difference count, removing the need for subtraction as described in method (ii).

The invention has been described with reference to specific exemplary embodiments thereof Various modification and changes may be made thereunto without departing from the broad spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense; the invention is limited only by the provided claims.

What is claimed is:

1. A method for displaying interlaced video data on a non-interlaced monitor, the interlaced video data comprising a plurality of paired fields, each pair of fields being vertically offset relative to each other by one-half of a field line spacing distance, each field comprising a plurality of lines of video data, the method including:

(a) capturing a first field and a second field of each pair of fields into respective buffers;

(b) scaling each of the first field and second field of each pair of fields to fill vertical resolution of the non-interlaced monitor;

(c) adjusting one of the first field or second field of the pair of fields to substantially correct for the vertical offset between the pairs of fields, where said adjusting is performed concurrently with said scaling;

(d) displaying the first field of each pair of fields on the non-interlaced monitor in a first time period; and

(e) displaying the second field of each pair of fields on the non-interlaced monitor in a second time period subsequent to the first time period.

2. The method of claim **1**, wherein scaling is achieved by line replication.

3. The method of claim **1**, wherein scaling is achieved by line dropping.

4. The method of claim **1**, wherein scaling is achieved by vertical interpolation between at least adjacent lines in the field being scaled.

5. The method claim **1**, wherein the scaling step includes scaling to a size other than two times the size of the interlaced video data by interpolating the video data.

6. The method of claim **1**, wherein the step of scaling is performed before the step of adjusting.

7. The method of claim **1**, wherein the step of scaling is performed after the step of adjusting.

8. The method of claim **1**, wherein the adjusting step includes changing display positions of one of the scaled first field or scaled second field by one or more lines on the noninterlaced monitor.

9. The method of claim **1**, wherein the adjusting step is achieved by vertical interpolation between at least adjacent lines in the field being adjusted.

10. A method for displaying interlaced video data on a non-interlaced monitor, the interlaced video data comprising a plurality of paired fields and having a field rate, each field comprising a plurality of lines of video data, the non-interlaced monitor having a variable frame display rate and a maximum frame display rate, the method including:

(a) capturing a first field and a second field of each pair of fields into distinct respective buffers at the interlaced video data field rate;

(b) scaling each of the first field and second field of each pair of fields to fill vertical resolution of the non-interlaced monitor;

(c) adjusting one of the first field or second field of the pair of fields to substantially correct for the vertical offset between the pairs of fields;

(d) setting the frame display rate of the non-interlaced monitor to a multiple of the field rate of the interlaced video data, such that the set frame display rate is no greater than the maximum frame display rate of the non-interlaced monitor;

(e) locking the first field and the second field of each pair of fields to the set frame display rate, where said locking includes determining a difference in field rate of the interlaced video data and the set frame display rate of the displayed first field and second field by sampling an input line counter and an output line counter; and

(f) sequentially displaying the first field and the second field on the non-interlaced monitor at the set frame display rate, such that each of the first field and second field are displayed for a predetermined number of frame times of the non-interlaced monitor.

11. The method of claim **10**, wherein the set frame display rate is a sub-multiple of the field rate of the interlaced video data.

12. The method of claim **10**, wherein the set frame display rate is a multiple of the field rate of the interlaced video data.

13. The method of claim **10**, wherein the locking step includes the step of adding or removing one or more lines in a vertical blanking region of the interlaced video data.

14. The method of claim **10**, wherein the locking step includes the step of increasing or decreasing the length of one or more lines in a vertical blanking region of the interlaced video data.

15. The method of claim **10**, wherein the locking step includes the step of adjusting the frequency of a clock used to generate the set frame display rate.

16. The method of claim **10**, wherein the locking step includes sensing drift in relative positions between lines in the interlaced video data and the displayed first field and second field.

17. The method of claim **10**, wherein said locking includes determining a difference in field rate of the interlaced video data and the set frame display rate of the displayed first field and second field by use of a difference counter.

18. A method for displaying interlaced video data on a non-interlaced monitor, the interlaced video data comprising a plurality of paired fields and having a field rate, each field comprising a plurality of lines of video data, the non-interlaced monitor having a variable frame display rate and a maximum frame display rate, the method including:

(a) capturing a first field and a second field of each pair of fields into distinct respective buffers at the interlaced video data field rate;

(b) scaling each of the first field and second field of each pair of fields to fill vertical resolution of the non-interlaced monitor;

(c) adjusting one of the first field or second field of the pair of fields to substantially correct for the vertical offset between the pairs of fields;

(d) setting the frame display rate of the non-interlaced monitor to a multiple of the field rate of the interlaced video data, such that the set frame display rate is no greater than the maximum frame display rate of the non-interlaced monitor;

(e) locking the first field and the second field of each pair of fields to the set frame display rate, where said locking includes determining a difference in the field rate of the interlaced video data and the set frame display rate of the displayed first field and second field by sampling a line video position within at least one of the first field and second field at a consistent time in an output monitor display cycle; and

(f) sequentially displaying the first field and the second field on the non-interlaced monitor at the set frame display rate, such that each of the first field and second field are displayed for a predetermined number of frame times of the non-interlaced monitor.

* * * * *

EXHIBIT B

US005847774A

United States Patent [19]

Cho

[11] Patent Number: 5,847,774

[45] Date of Patent: Dec. 8, 1998

[54] VIDEO SIGNAL PEAKING CIRCUIT

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[73] Assignee: **Daewoo Electronics Co., Ltd.**, Seoul, Rep. of Korea

[21] Appl. No.: **821,759**

[22] Filed: **Mar. 20, 1997**

[30] **Foreign Application Priority Data**

Oct. 29, 1996 [KR] Rep. of Korea 1996-49819

[51] **Int. Cl.**[6] **H04N 5/21**

[52] **U.S. Cl.** **348/625**; 348/627; 348/630; 348/678

[58] **Field of Search** 358/625, 627, 358/630, 631, 707, 678, 665–667, 668–669; H04N 5/21

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Primary Examiner—Andrew I. Faile
Assistant Examiner—Reuben M. Brown
Attorney, Agent, or Firm—Pillsbury Madison & Sutro LLP

[57] **ABSTRACT**

A circuit for peaking video signals, which can be developed by combining a video signal with a peaking signal having a preshooting and a overshooting potion that are respectively controlled in peaking levels thereof. The circuit includes a delay circuit for delaying a luminance signal for a first predetermined time in order to generate a first delayed signal and for delaying the first delayed signal for a second predetermined time in order to generate a second delayed signal. An adder adds the second delayed signal to a current video signal in order to generate an added signal. A variable amplifying section amplifies the added signal in response to a first control signal from an exterior in order to generate a first variable amplified signal, and amplifies the added signal in response to a second control signal from the exterior in order to generate a second variable amplified signal. A selecting section compares the added signal from the adder with a reference signal, and selects the first amplified signal or the second amplified signal according to the comparison result. A subtracter subtracts the first amplified signal or the second amplified signal from the select section from the first delayed signal from the delay section in order to generate a subtracted signal as a peaked video signal. Therefore, the circuit can control the preshooting portion and the overshooting portion of the peaking signal used to peak video signals.

10 Claims, 3 Drawing Sheets

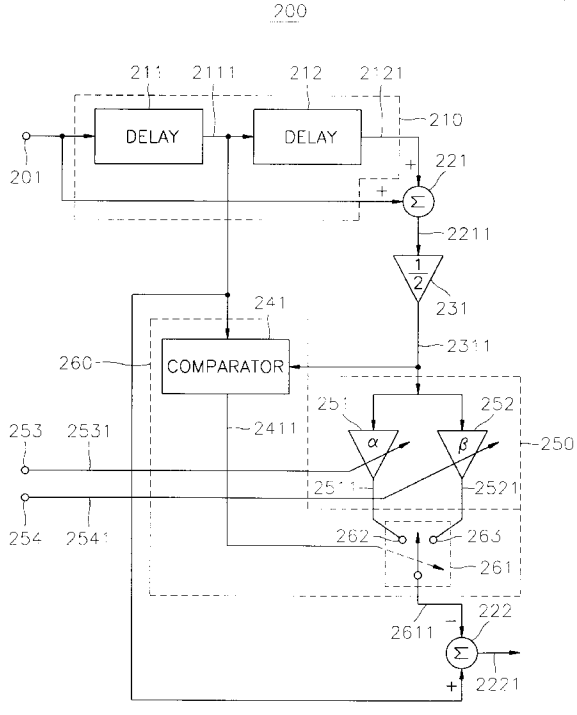


FIG. 1
(PRIOR ART)

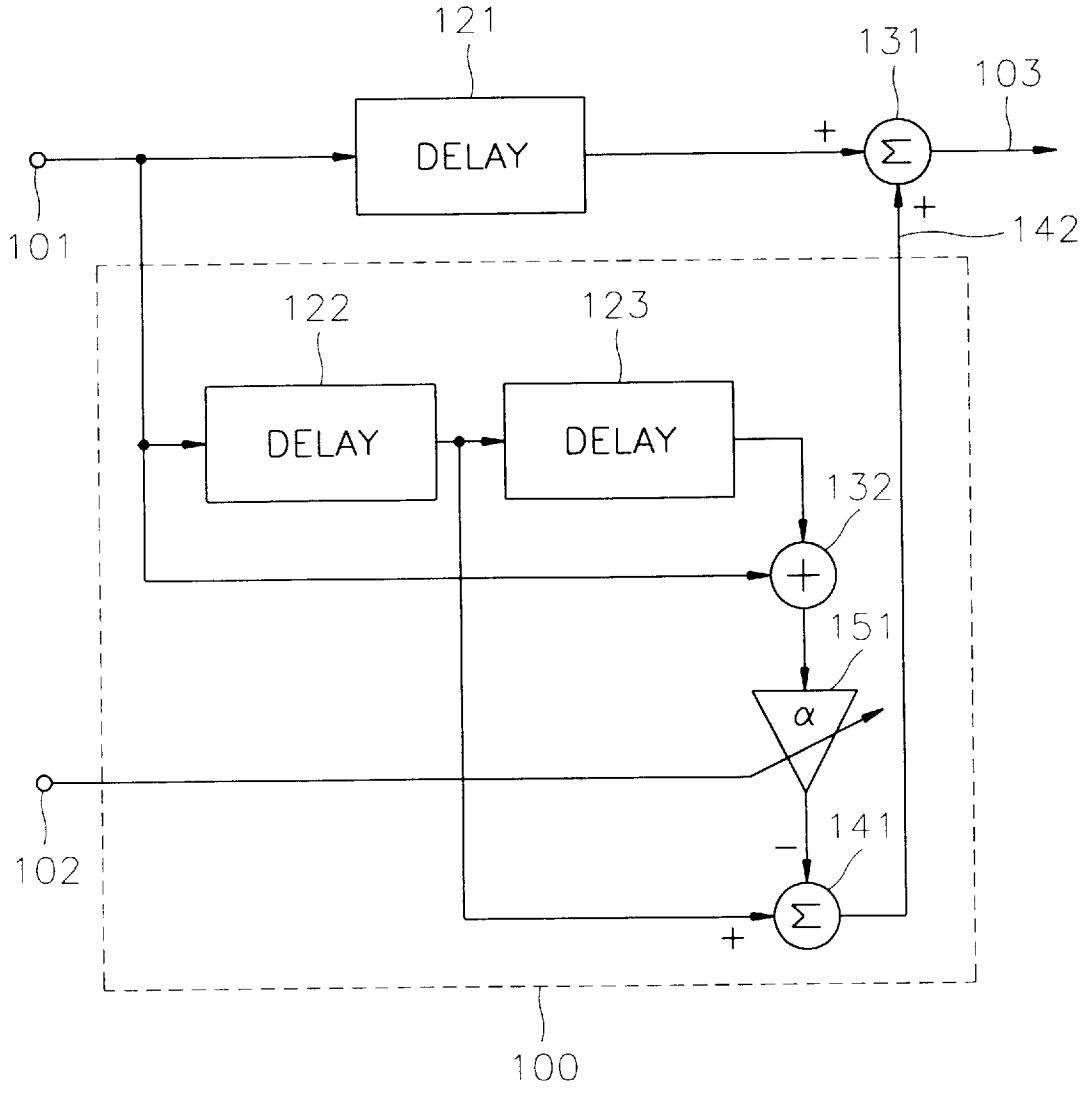
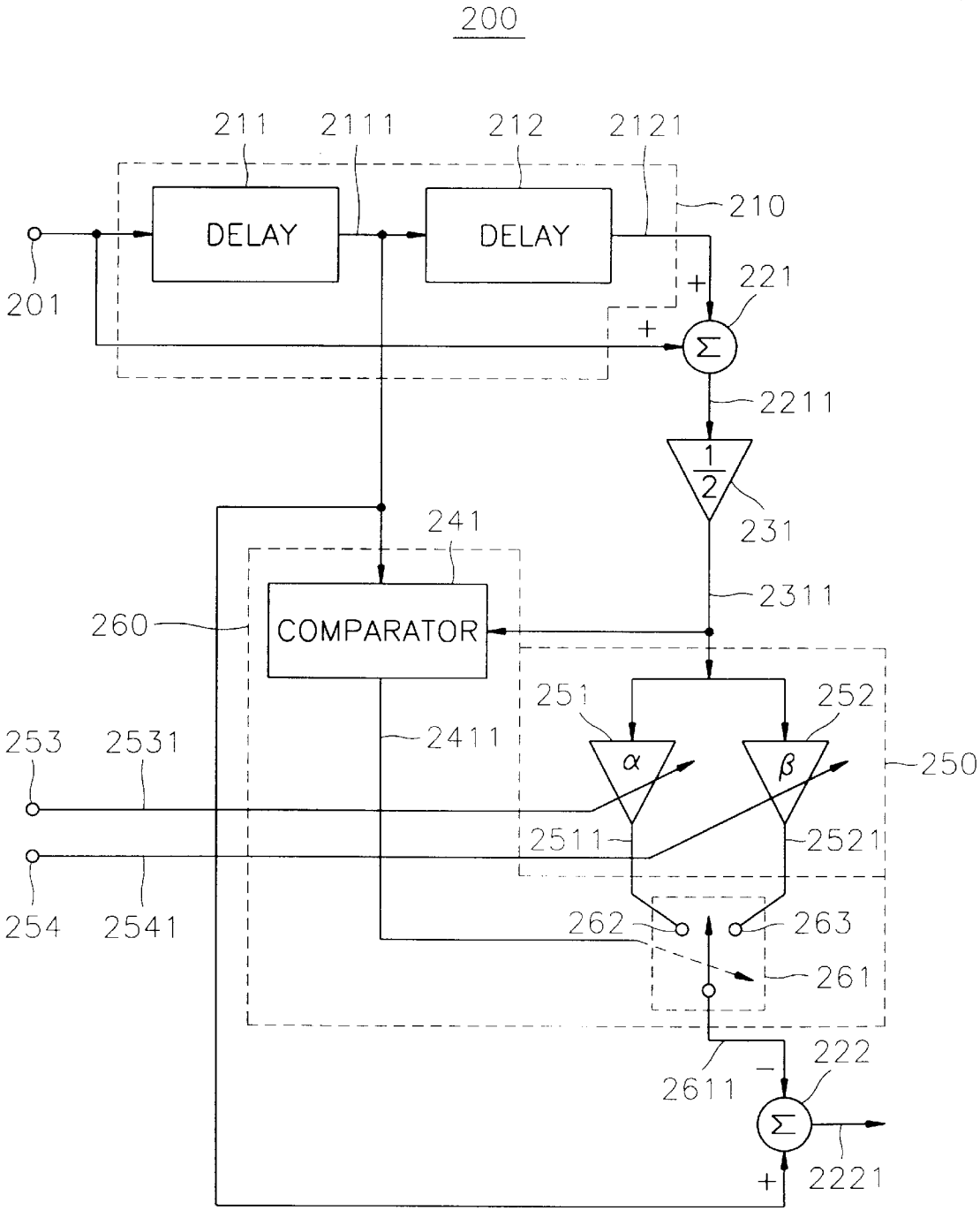


FIG. 2



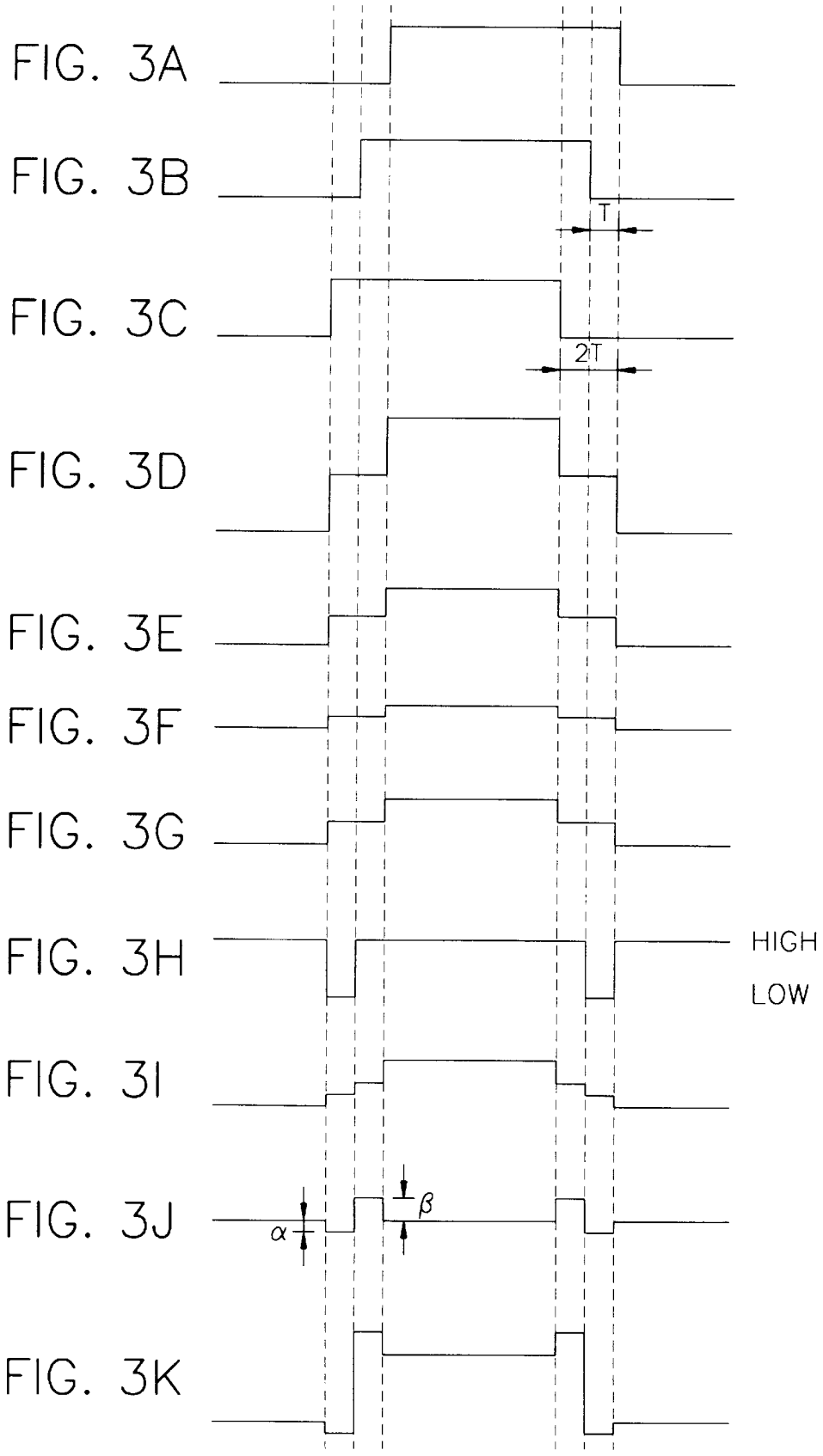


FIG. 3A
FIG. 3B
T
FIG. 3C
2T
FIG. 3D
FIG. 3E
FIG. 3F
FIG. 3G
FIG. 3H
HIGH
LOW
FIG. 3I
FIG. 3J
α
β
FIG. 3K

VIDEO SIGNAL PEAKING CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a circuit for a television system. More particularly, the present invention relates to a video signal peaking circuit for producing a peaking signal, which is added to a video signal in order to enhance an image displayed in a television receiver.

2. Description of the Prior Art

It is known that the response of a video signal processing system, such as one found in a television receiver, may be subjectively improved by increasing the slope or "steepness" of a video signal amplitude transition. The response may also be improved by generating a signal "preshoot" just before an amplitude transition, and a signal "overshoot" just after the amplitude transition, so that black-to-white and white-to-black transitions are accentuated.

FIG. **1** is a block diagram for showing a conventional circuit for peaking video signals. In FIG. **1**, the circuit includes a first delay section **121**, a second delay section **122**, a third delay section **123**, a first adder **131**, a second adder **132**, a subtracter **141**, and a variable amplifier **151**.

First and second delay sections **121** and **122** delay luminance signals which are continuously inputted through an input terminal **101** for a predetermined time T, respectively.

The delayed signals which are produced by first and second delay section **121** and **122** are respectively outputted to first adder **131** and subtracter **151**. Third delay **132** delays the time T delayed luminance signals from second delay section **122** for the time T in order to generate a luminance signal delayed for time 2T. Second adder **132** adds the 2T time delayed luminance signal to a current luminance signal through input terminal **101** so that second adder **132** generates continuously added luminance signals, and second adder **132** provides the added luminance signals to variable amplifier **151**. Variable amplifier **151** amplifies the added luminance signals in response to a control signal through a control signal input terminal **102** to generate amplified signals. The amplified signals generated by variable amplifier **151** are provided to subtracter **141**. Subtracter **141** subtracts the amplified signals from the T time delayed luminance signals in order to generate subtracted signals which are outputted to first adder **131** as peaking signals. First adder **131** adds the peaking signals from subtracter **141** to the T time delayed luminance signal to generate peaked luminance signals, and outputs the peaked luminance signals to a matrix circuit (not shown) through an output terminal **103**.

In the video signal peaking circuit **100**, as the amplifying degree of the variable amplifier **150** is controlled by the control signal, the peaking signal **142** from the subtracter **141** is controlled, so that the degree of the peaking luminance signals is controlled.

However, in the video signal peaking circuit **100**, when luminance signals are peaked by the control signal, the degree of preshooting and overshooting of the luminance signals is controlled at one level.

U.S. Pat. No. 4,350,995 (issued to Wayne E. Harlan on Sep. 21, 1982) discloses one example of an circuit for peaking video signals. The circuit disclosed in the above U.S. Patent includes a differential amplifier which produces a peaking component at an output, and a signal delay line for determining the frequency at which maximum peaking occurs. The delay line input is coupled to a source of video signals to be peaked and to one input of the delay line output is coupled to another input of the differential amplifier and to a signal combining point. A peaked video signal is produced by combining the peaking component from the differential amplifier with the delayed signal from the delay line. The operating parameters of the peaking circuit are established with respect to a normally expected range of video signal amplitude transitions so that the differential amplifier exhibits a linear response for transient or aperiodic transitions throughout the amplitude transition range. However, the differential amplifier exhibits a non-linear response for periodic transitions recurring at the maximum peaking frequency and having a magnitude greater than half the maximum transition magnitude of the range.

However, in the circuit, the degree of the peaking video signals is controlled at one level in both the preshooting and the overshooting.

For the foregoing reasons, there is need for a video signal peaking circuit that can respectively control peaking levels of the preshooting and the overshooting.

SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a video signal peaking circuit which is able to respectively control the preshooting and overshooting in peaking video signals.

In order to achieve the above-mentioned object of the present invention, there is provided a video signal peaking circuit, the video signal peaking circuit comprises:

- a delay section for delaying a luminance signal for a first predetermined time in order to generate a first delayed signal and for delaying the first delayed signal for a second predetermined time in order to generate a second delayed signal;
- an adder for adding the second delayed signal to a current video signal in order to generate an added signal;
- a variable amplifying section for amplifying the added signal in response to a first control signal from an exterior in order to generate a first variable amplified signal, and amplifying the added signal in response to a second control signal from the exterior in order to generate a second variable amplified signal;
- a selecting section for comparing the added signal from said adder with a reference signal, and for selecting the first amplified signal or the second amplified signal according to the comparison result; and
- a subtracter for subtracting the first amplified signal or the second amplified signal from said select section from the first delayed signal from said delay section in order to generate a subtracted signal as a peaked video signal.

According to the present invention, the video signal peaking circuit can respectively control the degree of the preshooting and the overshooting portion of the peaking signal used to peak video signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings, in which:

FIG. **1** is a block diagram of a conventional video signal peaking circuit;

FIG. **2** is a block diagram of a video signal peaking circuit according to the present invention; and

FIGS. **3**A through **3**K are waveform diagrams for showing the operations at serveral portions of the video signal peaking circuit of FIG. **2**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A description will be given below in detail, with reference to the accompanying drawings, of the circuitry configuration and the operation of the circuitry according to one embodiment of the present invention.

FIG. **2** shows a video signal peaking circuit **200** according to one embodiment of the invention. In FIG. **2**, the video signal peaking circuit **200** includes a delay circuit **210**, an adder **221**, a variable amplifying section **250**, a selection section **260**, and a subtracter **222**.

Delay circuit **210** consists of a first delay section **211** and a second delay section **212**. First delay section **211** delays a luminance signal which is inputted through a luminance signal input terminal **201** for a predetermined time T so that a first delayed signal **2111** is generated at an output terminal therein. The first delayed signal **2111** generated by first delay section **211** is provided to second delay section **212** and selection section **260**. Second delay section **212** delays the first delayed signal for a predetermined time which is preferably time T, thereby generating a second delayed signal **2121** delayed for time 2T. The second delayed signal **2121** is provided to adder **221**.

Adder **221** adds the second delayed signal from second delay section **212** to a current luminance signal through the luminance signal input terminal **201** to generate an added signal **2211**, which is provided to a one-half amplifier **231**. One-half amplifier **231** amplifies the added signal **2211** to develop an ½ amplified signal **2311** and outputs the ½ amplified signal **2311** to variable amplifying section **250** and selection section **260**.

Variable amplifying section **250** includes a first variable amplifier **251** and a second variable amplifier **252**. First variable amplifier **251** amplifies the ½ amplified signal **2311** from one-half amplifier **231** in response to a first control signal **2531** which is provided from an exterior through a first control input terminal **253**, thereby generating a first variable amplified signal **2511**. Second variable amplifier **252** amplifies ½ amplified signal **2311** from one-half amplifier **231** in response to a second control signal **2541** which is provided from the exterior through a second control input terminal **254**, thereby generating a second variable amplified signal **2521**.

The selection section **260** selectively outputs first or second variable amplified signal **2511** and **2521** based on ½ amplified signal **2311** of one-half amplifier **231**. Selection section **260** preferably includes a comparator **241** and a switch **261** for selectively outputting the first or the second variable amplified signal **2511** or **2521**. The comparator **241** compares a voltage level of ½ amplified signal **2311** with the voltage level of a reference signal provided from the exterior, preferably the first delayed signal **2111** from first delay section **2111**, and provides the comparison result thereof to the switch **261** so as to control a switching operation of the switch **261**. Switch **261** is operated according to comparison result **2411** provided from comparator **241**, thereby selecting one of first and second variable amplified signals **2511** and **2521** and outputting the selected signal by switching to the subtractor **222**.

Subtractor **222** subtracts first or second variable amplified signals **2511** or **2521** provided from switch **261** from first delayed signal **2111** provided from first delay section **211**, thereby developing a peaking signal **2221**.

The operation of the embodiment according to the invention is described in detail with reference to FIGS. **2** and **3**A through **3**K.

In FIG. **2**, when a luminance signal, which has a waveform as shown in FIG. **3**A and is separated by a luminance and chroma signal separating apparatus (not shown), is provided to first delay section **211** through luminance signal input terminal **201**, first delay section **211** delays the inputted luminance signal for the predetermined time T to generate a first delayed signal **2111**, as shown in FIG. **3**B, and provides first delayed signal **2111** to second delay **212**, comparator **241**, and subtracter **222**.

Second delay section **212** delays once more first delayed signal **2111** for the predetermined time T, in the same manner as the operation of first delay section **212** to generate second delayed signal **2121**, as shown in FIG. **3**C, and provides second delayed signal **2121** to adder **221**. Adder **221** adds second delayed signal **2121** to a current luminance signal through luminance input terminal **201** to generate an added signal **2211**, as shown in FIG. **3**D, and provides one-half amplifier **231** with added signal **2211**.

One-half amplifier **231** amplifies added signal **2211** from adder **221** at the rate of one-half to generate a ½ amplified signal **2311**, as shown in FIG. **3**E, and provides ½ amplified signal **2311** to comparator **241**, first variable amplifier **251**, and second variable amplifier **252**.

First variable amplifier **251** amplifies ½ amplified signal **2311** from one-half amplifier **231** in response to first control signal **2531** through first control input terminal **253**, thereby generating first amplified signal **2511**, and provides first amplified signal **2511** to a first input terminal **262** of the switch **261**. For example, when ½-amplified signal **2311**, as shown in FIG. **3**E, generated by one-half amplifier **231** is inputted to first variable amplifier **251**, and the rate of amplifying of the first variable amplifier **251** is one-fifth, the first variable amplifier ⅕-amplifies the ½-amplified signal and outputs a ⅕-amplified signal as first amplified signal **2511** to first input terminal **262** of switch **261**.

Further, second variable amplifier **252** amplifies ½-amplified signal from one-half amplifier **231** in response to the second control signal through second input terminal **254** to generate a second amplified signal **2521**, and provides second amplified signal **2521** to a second input terminal **263** of switch **261**. For example, when ½-amplified signal **2311**, which has a waveform as shown in FIG. **3**E, and is generated by one-half amplifier **231** is inputted to second variable amplifier **252**, and the rate of amplifying of the second variable amplifier **252** is four-fifths, the second variable amplifier **4**/**5**-amplifies ½-amplified signal **2311** and outputs a ⅘-amplified signal as second amplified signal **2521** to second input terminal **263** of switch **261**.

Comparator **241** compares ½-amplified signal **2311** from one-half amplifier **231** with first delayed signal **2111** from first delay **211** to generate a signal of the comparison result, and provides the signal of the comparing result for switch **261** to control switch **261**. For example, when a first delay signal, which has a waveform as shown in FIG. **3**B and is from first delay **211**, and an ½-amplified signal, as shown in FIG. **3**E, from one-half amplifier **231** are respectively inputted to both input terminals of comparator **241**, comparator **241** outputs a logic signal as a signal to control switch **261**. The logic signal outputted from comparator **241** is depicted in FIG. **3**H. That is, when the level of first delayed signal **2111** is lower than that of ½-amplified signal **2311**, comparator **241** provides a low logic signal to switch **261**. In contrast, when the level of first delayed signal **2111** is higher

than that of ½-amplified signal **2311**, comparator **241** provides the high logic signal to switch **261**.

Switch **261** operates in response to the logic state of the logic signal provided from comparator **241** so that switch **261** selectively outputs first amplified signal **2511** or second amplified signal **2521** to the subtracter **222**. For example, when a low logic signal **2411** from comparator **241** is provided to switch **261**, switch **261** switches on first input terminal **262** thereof thereby outputting first amplified signal **2511** from first variable amplifier **251** to subtracter **222**. In contrast, when a high logic signal from comparator **241** is provided to switch **261**, switch **261** switches on second input terminal **263** thereof, thereby outputting second amplified signal **2521** from second variable amplifier **252** to subtracter **222**.

FIG. **3**I is a waveform of the signal which is outputted from the switch **261** when first amplified signal **2511** as shown in FIG. **3**F, second amplified signal **2521** having a waveform as shown in FIG. **3**G, and the logic signal which is a comparing result of comparator **241** depicted in FIG. **3**H, are respectively inputted to switch **261**.

When signal **2611**, which has a waveform as shown in FIG. **3**I and is developed by switch **261**, is provided to subtracter **222**, subtracter **222** subtracts signal **2611** from first delayed signal **2111**, which is provided from first delay **211**, so that a peaking signal **2221**, as shown in FIG. **3**J, is developed.

The peaking signal of FIG. **3**J has a preshooting portion (α) and a overshooting portion (β) which can be controlled according to each amplification rates of first variable amplifier **251** and second variable amplifier **252**, respectively.

Peaking signal **2221**, which is shown in FIG. **3**J, and is generated by subtracter **222**, is added to a delayed signal, which is preferably second delayed signal **2121** generated by the second delay section **212** so as to generate a peaked video signal such as the one shown in FIG. **3**K. Therefore, by the embodiment of the present invention, each of the degrees of the preshooting and the overshooting portion of the peaking signal which is used to peak video signal can be controlled.

As described previously, the present invention has an advantage that it can control the preshooting portion and the overshooting portion of the peaking signal used to peak video signals.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiment is therefore to be considered in all respects as illustrative and not respective, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and the range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed is:

1. A circuit for peaking video signals, said circuit comprising:

a delay section for delaying a luminance signal for a first predetermined time in order to generate a first delayed signal and for delaying the first delayed signal for a second predetermined time in order to generate a second delayed signal;

an adder for adding the second delayed signal to a current video signal in order to generate an added signal;

a variable amplifying section for amplifying the added signal in response to a first control signal from an exterior in order to generate a first variable amplified signal, and amplifying the added signal in response to a second control signal from the exterior in order to generate a second variable amplified signal;

a selecting section for comparing the added signal from said adder with a reference signal, and for selecting the first amplified signal or the second amplified signal according to the comparison result; and

a subtracter for subtracting the first amplified signal or the second amplified signal from said select section from the first delayed signal from said delay section in order to generate a subtracted signal as a peaked video signal.

2. A circuit as recited in claim **1**, wherein said delay section includes a first delay section for delaying a video signal for the first predetermined time in order to generate the first delayed signal, and a second delay section for delaying the first delayed signal for the second predetermined time in order to generate the second delayed signal.

3. A circuit as recited in claim **1**, wherein said variable amplifying section includes a first variable amplifier for amplifying the added signal from said adder in response to the first control signal, and a second variable amplifier for amplifying the added signal from said adder in response to the second control signal.

4. A circuit as recited in claim **1**, wherein said selection section includes a comparator for comparing the added signal from said adder with the reference signal, and a switch for selecting the first variable amplified signal or the second variable amplified signal according to the comparison result.

5. A circuit as recited in claim **4**, wherein said comparator generates a high logic or a low logic signal according to the comparison result and provides said switch with the logic signal.

6. A circuit as recited in claim **1**, wherein the reference signal is the first delayed signal generated by said delay section.

7. A circuit as recited in claim **1**, further comprising: an amplifier for amplifying the added signal from said adder in order to generate an amplified signal, and for providing the amplified signal to said select section and said amplifying section.

8. A circuit for peaking video signals, said circuit comprising:

a first delay means for delaying an input luminance signal for a first predetermined time in order to generate a first delayed signal;

a second delay means for delaying the first delayed signal for a second predetermined time in order to generate a second delayed signal;

an adder for adding said second delayed signal to a current input luminance signal in order to generate an added signal;

a first amplifier for amplifying the added signal in order to generate a first amplified signal;

a comparator for comparing the first amplified signal from the first amplifier with a reference signal;

a first variable amplifier for amplifying the first amplified signal according to a first control signal in order to generate a second amplified signal;

a second variable amplifier for amplifying the first amplified signal according to a second control signal in order to generate a third amplified signal;

a switch for selecting the second or third amplified signal according to the comparison result in order to output the second or the third amplified signal; and

a subtracter for subtracting the second or third amplified signal selected by said switch from the first delay signal from said first delay means, thereby generating a subtracted signal as peaked video signal.

9. A circuit as recited in claim **8**, wherein said comparator generates a high logic signal or a low logic signal according to the comparison result and provides the high logic or the low logic signal to said switch.

10. A circuit as recited in claim **8**, wherein the reference signal is the first delay signal generated by said delay section.

* * * * *

EXHIBIT C

US006490250B1

(12) **United States Patent**
Hinchley et al.

(10) **Patent No.: US 6,490,250 B1**
(45) **Date of Patent: Dec. 3, 2002**

(54) **ELEMENTARY STREAM MULTIPLEXER**

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(73) Assignee: **Conexant Systems, Inc.**, Newport Beach, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Mar. 9, 1999**

(51) **Int. Cl.**[7] **H04J 3/14**; H04L 12/26
(52) **U.S. Cl.** **370/232**; 370/235; 370/465
(58) **Field of Search** 370/230, 231, 370/232, 233, 234, 235, 506, 537, 538, 545, 465; 725/148, 149; 709/231, 233, 234

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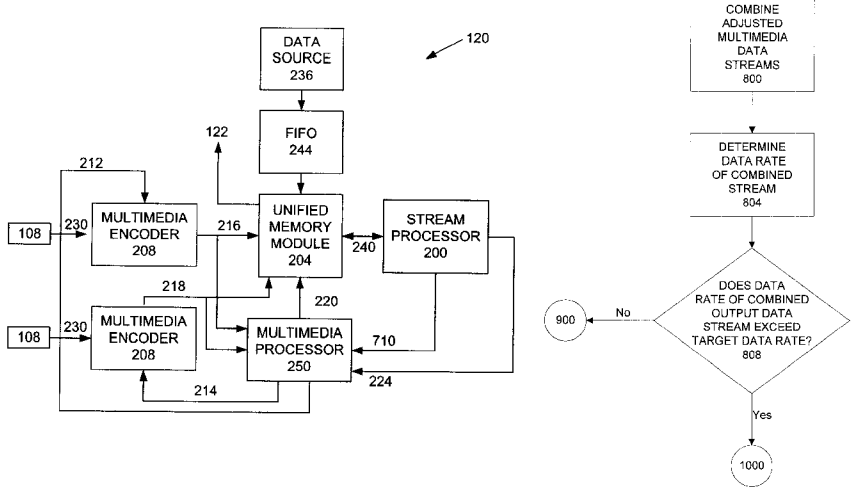
Primary Examiner—Hassan Kizou
Assistant Examiner—David Odland
(74) *Attorney, Agent, or Firm*—Thomas, Kayden, Horstemeyer & Risley, LLP

(57) **ABSTRACT**

An integrated multimedia encoding system is disclosed. Multimedia encoders which are capable of adjusting bit rates receive multimedia data to compress the data. After compressing the data, the multimedia encoders adjust the bit rates of the elementary streams responsive to a control input. Bit rates are increased or decreased using delays or, for video data, by allocating more or less bits to each macroblock, frame or group of frames. A unified memory module is coupled to the multimedia encoders to store the multimedia elementary stream data, the Program or Transport stream data, and data from other sources as needed. The unified memory is capable of adjusting storage allocations responsive to the realtime requirements of the incoming multimedia streams and the outgoing Program or Transport stream data. A stream processor is coupled to the unified memory module and the multimedia encoders for multiplexing the elementary streams into a single stream, and monitoring the actual bit rate of the combined multimedia stream. Monitoring the actual bit rate as a function of number of bits passed over a period of time provides accurate feedback as to the system throughput. A multimedia processor then determines the bit rates of the elementary streams, and generating a control signal to adjust the bit rates of the encoder to ensure that an optimal bit rate is continuously achieved by the system. The stream processor also operates using dedicated instructions which allow the stream processor to efficiently multiplex the incoming streams together.

14 Claims, 11 Drawing Sheets



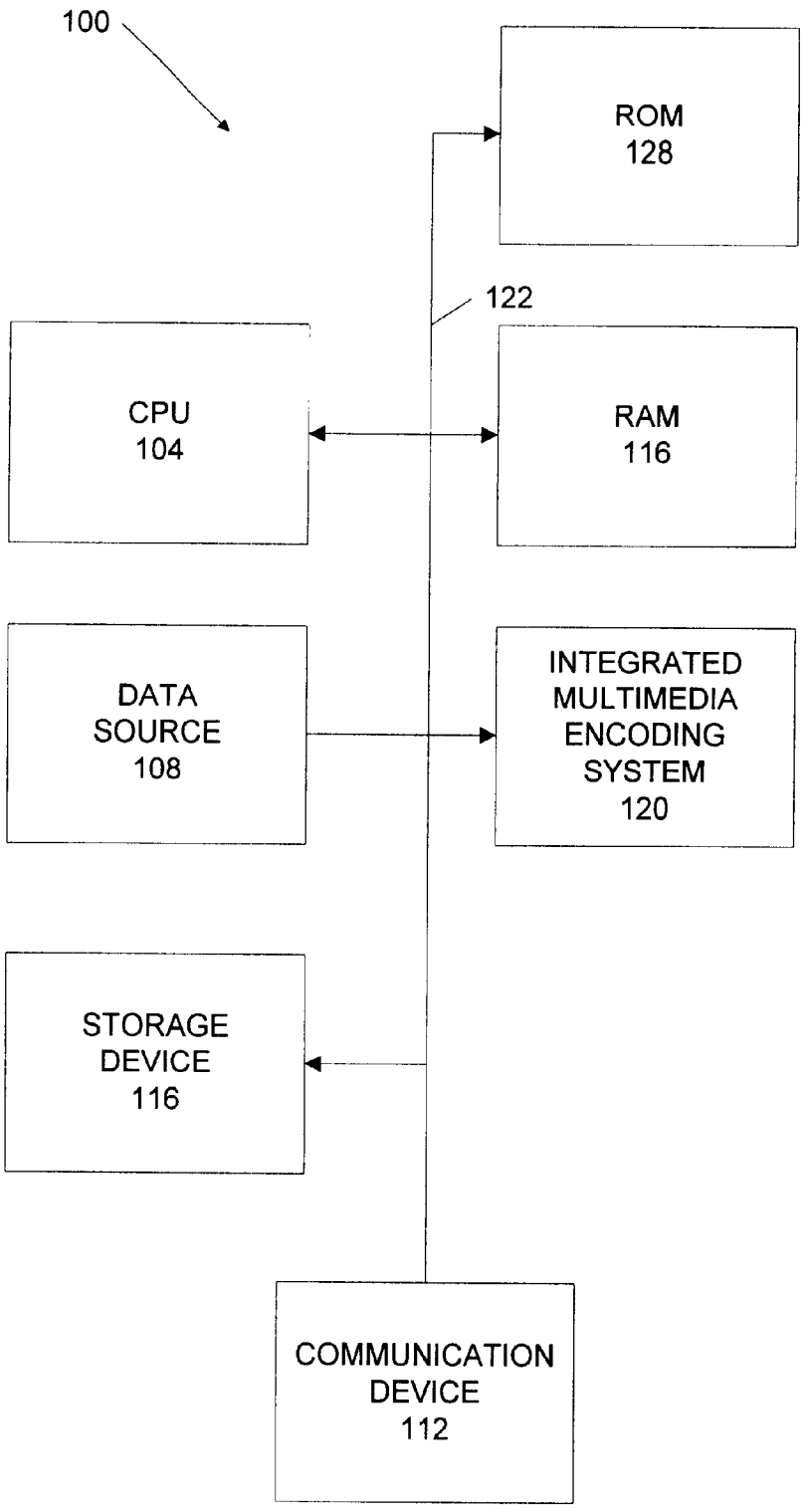

100
ROM
128
122
CPU
104
RAM
116
DATA
SOURCE
108
INTEGRATED
MULTIMEDIA
ENCODING
SYSTEM
120
STORAGE
DEVICE
116
COMMUNICATION
DEVICE
112

FIGURE 1

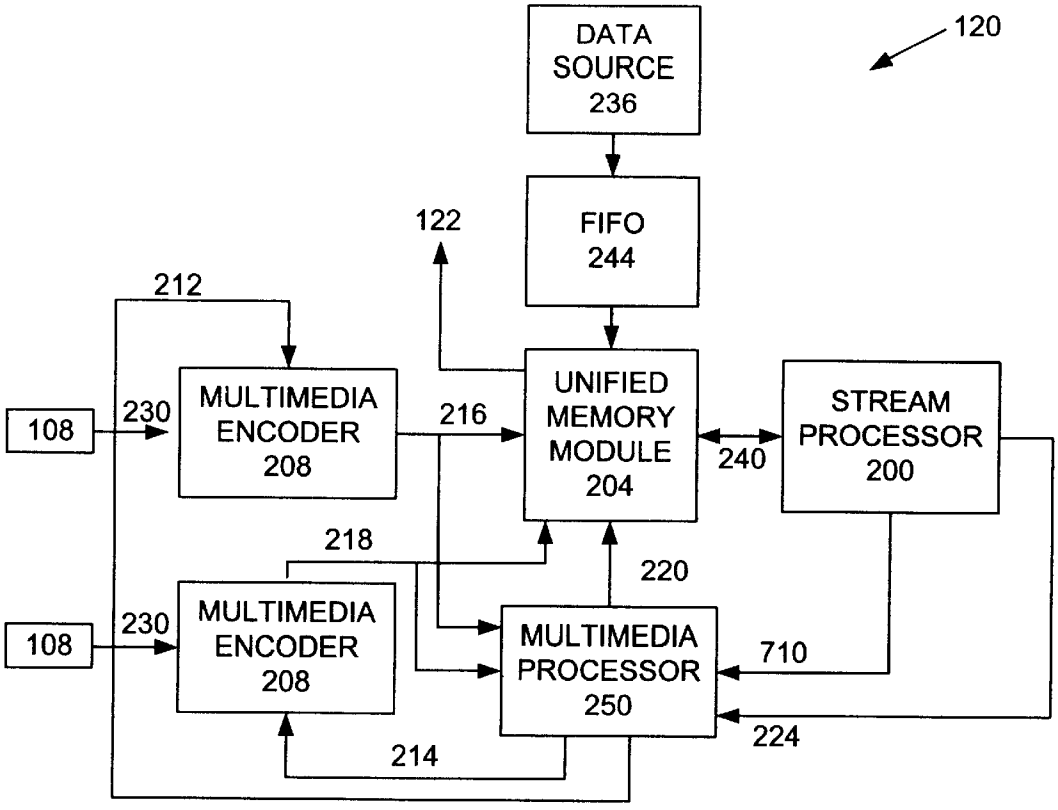


FIGURE 2

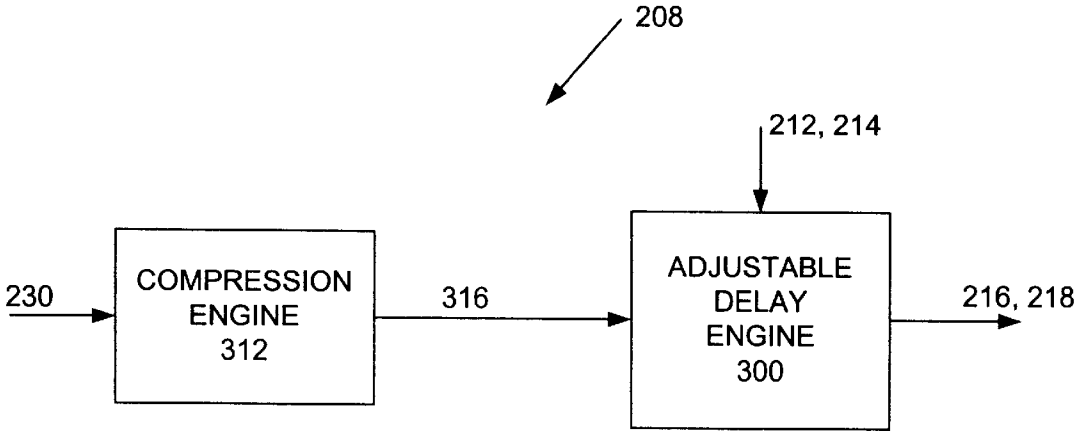


FIGURE 3

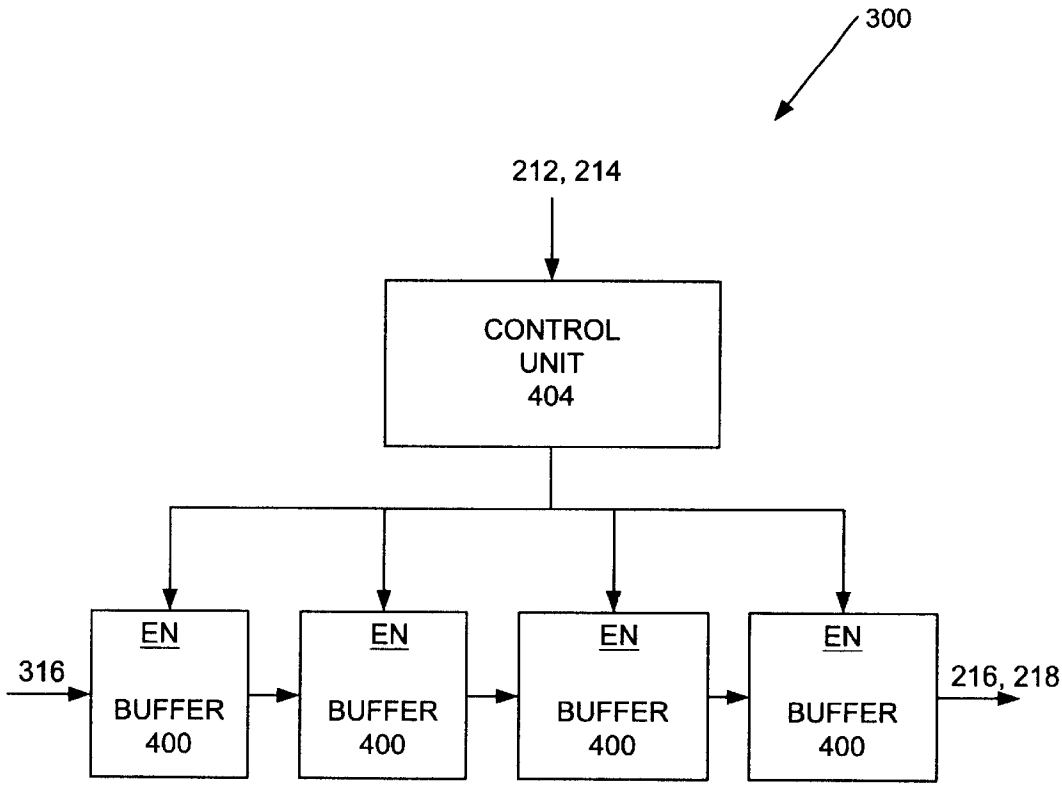

300
212, 214
CONTROL UNIT 404
316
EN
BUFFER 400
EN
BUFFER 400
EN
BUFFER 400
EN
BUFFER 400
216, 218

FIGURE 4

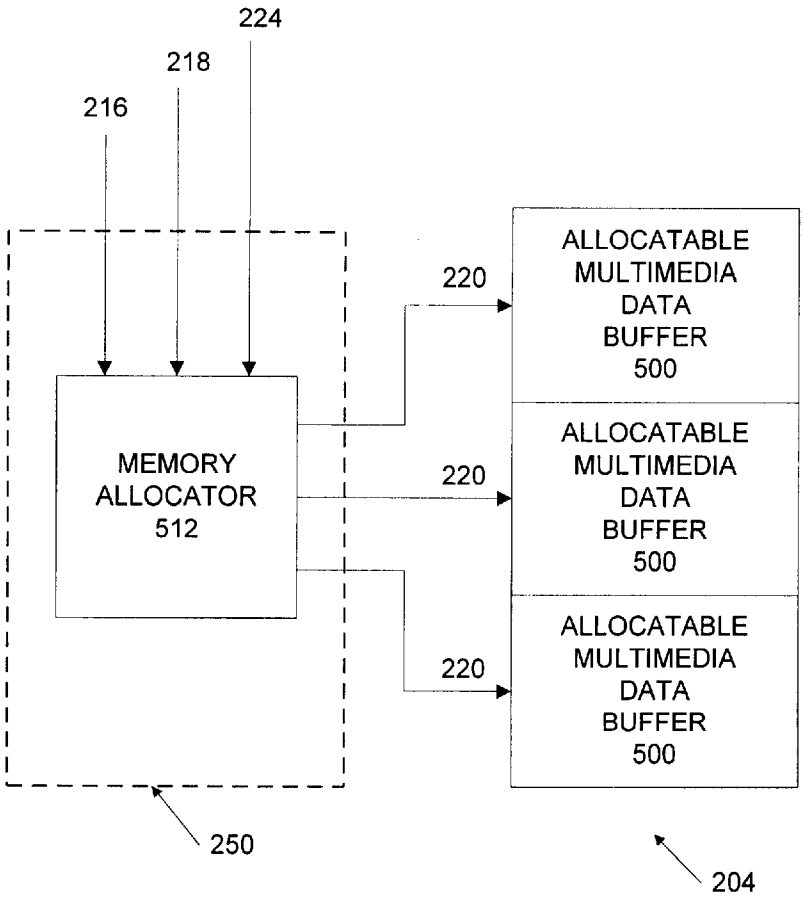

224
218
216
220
220
220
MEMORY ALLOCATOR 512
ALLOCATABLE MULTIMEDIA DATA BUFFER 500
ALLOCATABLE MULTIMEDIA DATA BUFFER 500
ALLOCATABLE MULTIMEDIA DATA BUFFER 500
250
204

FIGURE 5

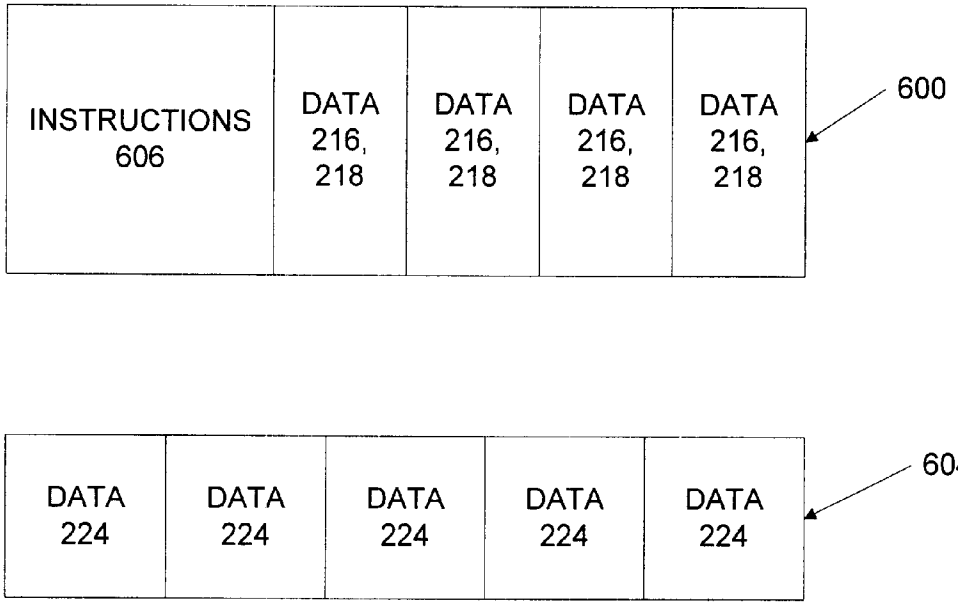

INSTRUCTIONS 606
DATA 216, 218
DATA 216, 218
DATA 216, 218
DATA 216, 218
600
DATA 224
DATA 224
DATA 224
DATA 224
DATA 224
604

FIGURE 6

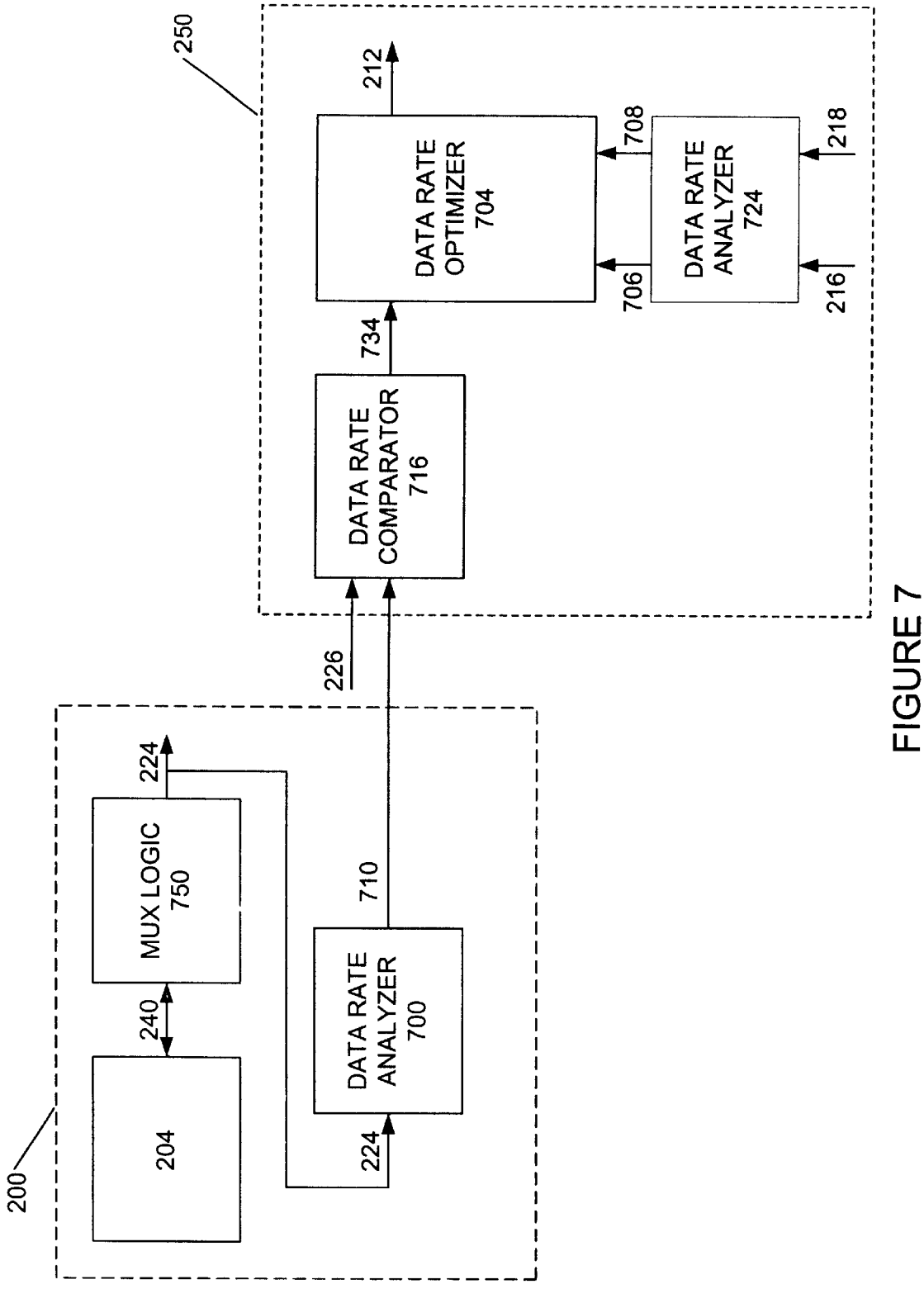

250
212
DATA RATE OPTIMIZER 704
708
706
DATA RATE ANALYZER 724
218
216
734
DATA RATE COMPARATOR 716
226
224
MUX LOGIC 750
240
204
710
DATA RATE ANALYZER 700
224
200

FIGURE 7

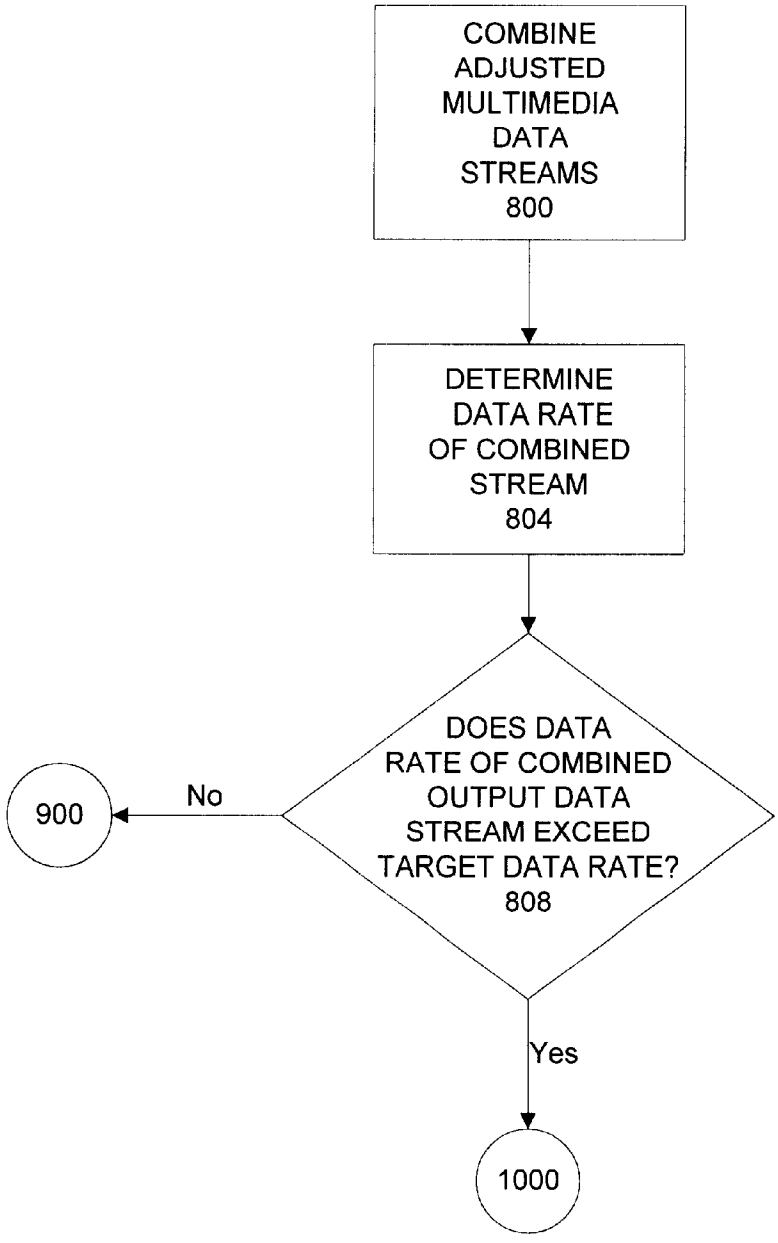

COMBINE ADJUSTED MULTIMEDIA DATA STREAMS 800
DETERMINE DATA RATE OF COMBINED STREAM 804
DOES DATA RATE OF COMBINED OUTPUT DATA STREAM EXCEED TARGET DATA RATE? 808
No
900
Yes
1000

FIGURE 8

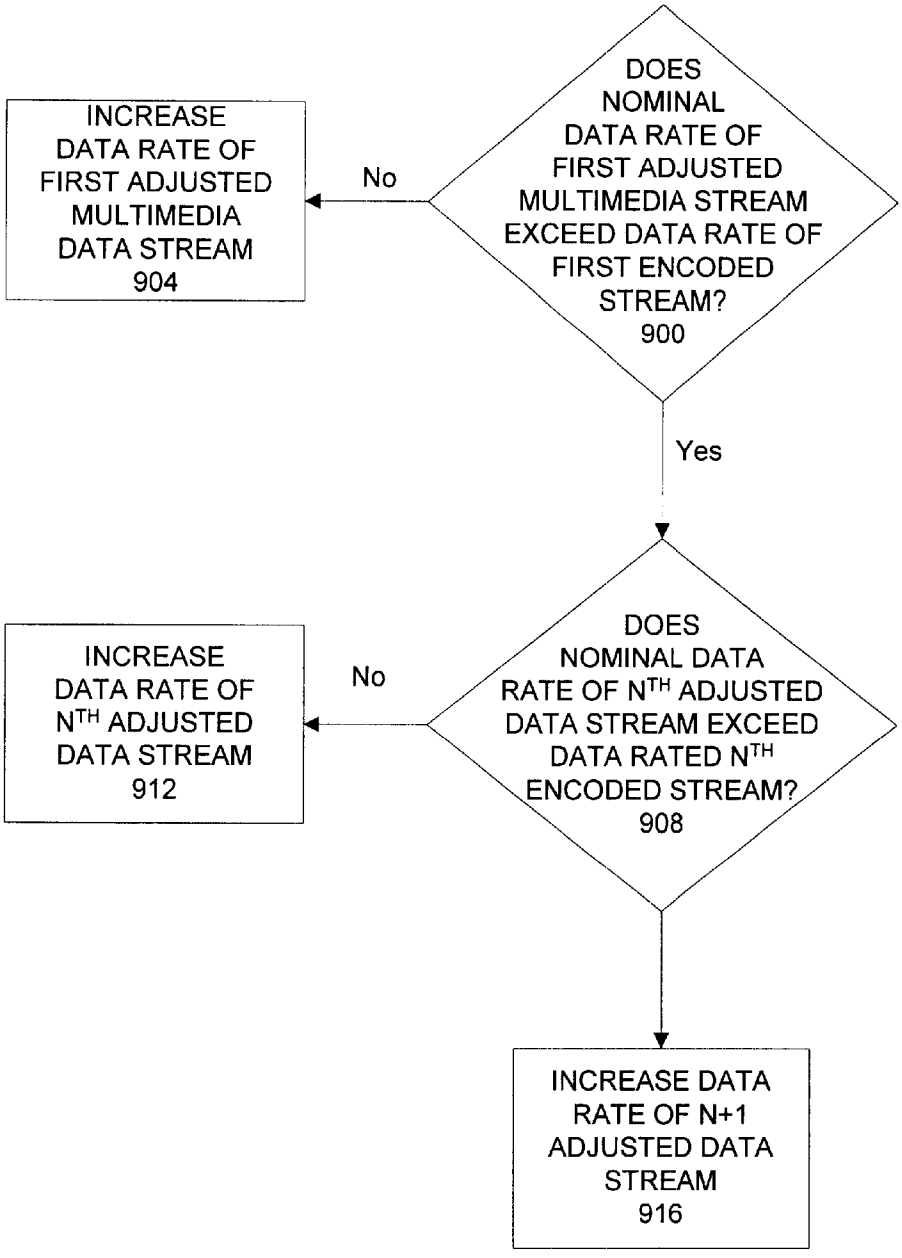

DOES NOMINAL DATA RATE OF FIRST ADJUSTED MULTIMEDIA STREAM EXCEED DATA RATE OF FIRST ENCODED STREAM? 900
No
INCREASE DATA RATE OF FIRST ADJUSTED MULTIMEDIA DATA STREAM 904
Yes
DOES NOMINAL DATA RATE OF N^TH ADJUSTED DATA STREAM EXCEED DATA RATED N^TH ENCODED STREAM? 908
No
INCREASE DATA RATE OF N^TH ADJUSTED DATA STREAM 912
INCREASE DATA RATE OF N+1 ADJUSTED DATA STREAM 916

FIGURE 9

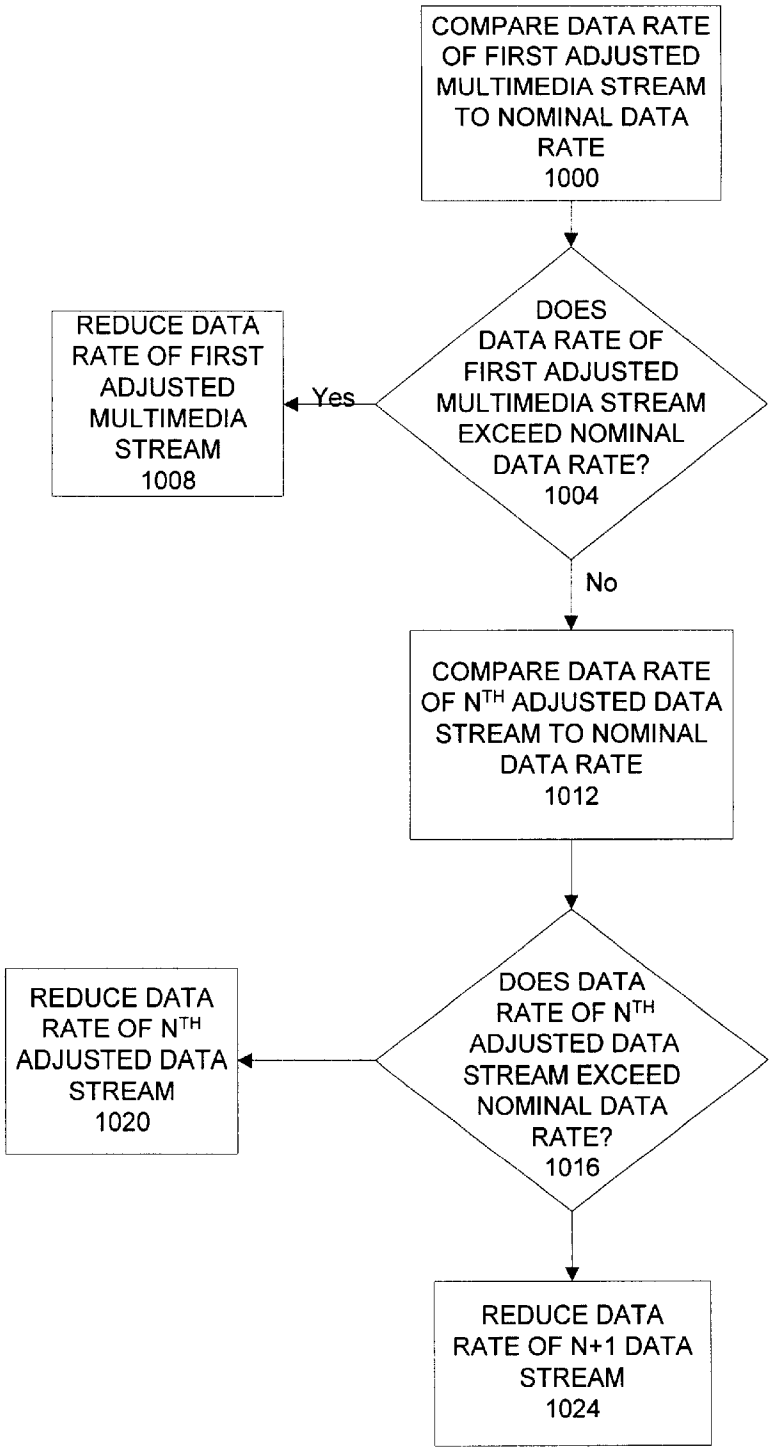


FIGURE 10

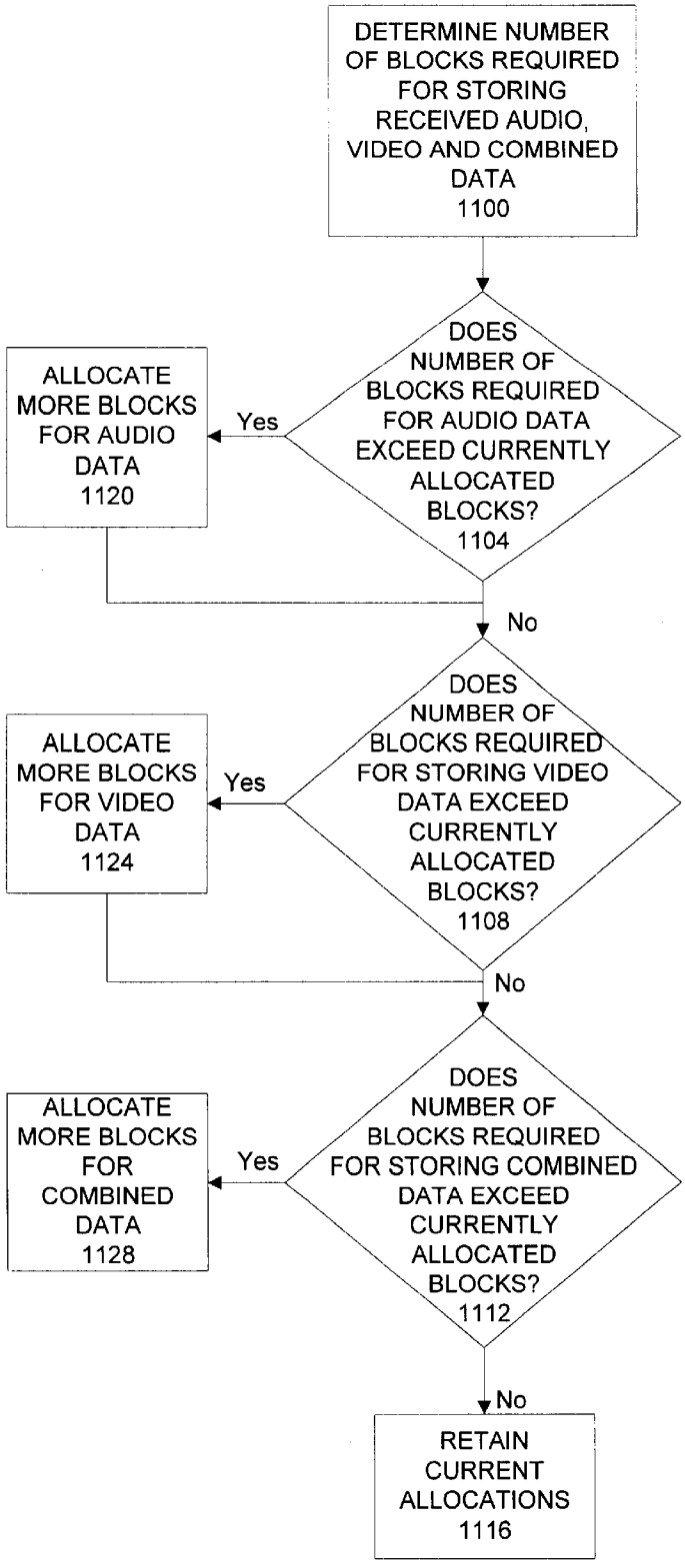


FIGURE 11

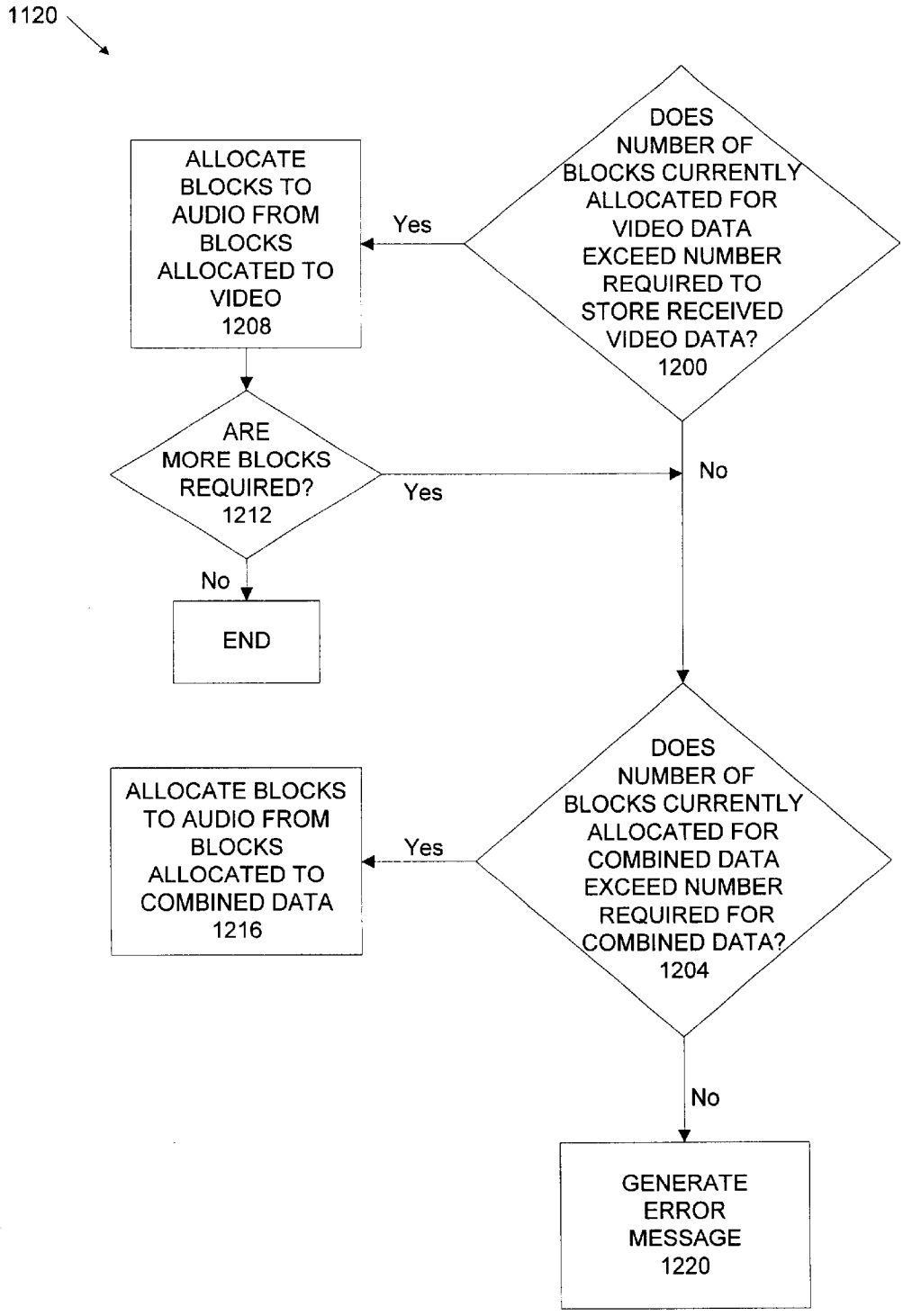

1120
DOES NUMBER OF BLOCKS CURRENTLY ALLOCATED FOR VIDEO DATA EXCEED NUMBER REQUIRED TO STORE RECEIVED VIDEO DATA? 1200
Yes
ALLOCATE BLOCKS TO AUDIO FROM BLOCKS ALLOCATED TO VIDEO 1208
ARE MORE BLOCKS REQUIRED? 1212
Yes
No
No
END
DOES NUMBER OF BLOCKS CURRENTLY ALLOCATED FOR COMBINED DATA EXCEED NUMBER REQUIRED FOR COMBINED DATA? 1204
Yes
ALLOCATE BLOCKS TO AUDIO FROM BLOCKS ALLOCATED TO COMBINED DATA 1216
No
GENERATE ERROR MESSAGE 1220

FIGURE 12

ELEMENTARY STREAM MULTIPLEXER

FIELD OF THE INVENTION

The application relates generally to multimedia encoders and specifically an integrated multimedia stream multiplexer.

BACKGROUND OF THE INVENTION

Multimedia encoders, such as those used for MPEG and MPEG2 encoding, provide the necessary compression to allow video and audio data to be transferred, stored, and played in a computer environment. Conventional MPEG encoders typically use two encoders, video and audio, which receive data transmitted from a data source. Each encoder is coupled to a separate memory for storing the video and audio data. The video encoder compresses the video data and transmits the compressed data to the conventional stream multiplexer controller. The audio encoder performs the same tasks and transmits the compressed audio data to the stream multiplexer controller. In an MPEG2 environment, the two elementary streams are multiplexed by the stream multiplexer controller to generate either a Program or Transport stream, depending on the embodiment. The Program or Transport stream are stored in a separate PS/TS memory, or are fed directly to another device, such as a communications link. In this conventional system, the stream multiplexer operates independently of the video and audio encoders, and therefore the output bit rate of the Program or Transport stream is unpredictable, as it will vary as the bit rates of the elementary streams vary. The unpredictable bit rate of the output stream makes it more difficult to process the Program or Transport stream downstream. Additionally, in conventional systems when the bit rate of one stream decreases, the bit rate of the Program or Transport stream may decrease correspondingly, thus lowering the system throughput unnecessarily. The use of independent memory for each encoder also leads to underutilization of system resources. When the bit rate of a stream decreases, less data is stored in the corresponding memory by the corresponding encoder. However, in conventional systems, the newly available storage space remains unused until the bit rate for the stream increases. Finally, conventional stream processors process incoming elementary streams using a predetermined ratio-based approach which restricts the granularity of the multiplexing as the ratios are fixed and cannot be optimized for the requirements of different output streams.

Therefore, an integrated multimedia encoding system which is capable of generating a program or transport stream at a bit rate at or near the maximum bit rate capacity for the system is needed. Additionally, an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed. Finally, a programmable elementary stream multiplexer is needed which takes advantage of dedicated instructions to perform the task of generating a single output data stream, and which is flexible to adjust the data rate for different formats.

SUMMARY OF THE INVENTION

In accordance with the present invention, an integrated multimedia encoding system is disclosed. Multimedia encoders which are capable of adjusting bit rates receive multimedia data to compress the data. After compressing the data, the multimedia encoders adjust the bit rates of the elementary streams responsive to a control input. Bit rates may be increased or decreased using delays, and generating more or less bits for each macroblock, frame or group of frames, or by increasing or decreasing the rate at which multimedia data is transmitted to the encoders. A unified memory module is coupled to the multimedia encoders to store the multimedia elementary stream data, the Program or Transport stream data, and data from other sources as needed. The unified memory is capable of adjusting storage allocations responsive to the realtime requirements of the incoming multimedia streams and the outgoing Program or Transport stream data. A stream processor is coupled to the unified memory module and the multimedia encoders for multiplexing the elementary streams into a single stream, and monitoring the actual bit rate of the combined multimedia stream. Monitoring the actual bit rate as a function of number of bits passed over a period of time provides accurate feedback as to the system throughput. A multimedia processor then determines the bit rates of the elementary streams, and generating a control signal to adjust the bit rates of the encoder to ensure that an optimal bit rate is continuously achieved by the system. The stream processor also operates using dedicated instructions which allow the stream processor to efficiently multiplex the incoming streams together.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an integrated multimedia encoding system in accordance with the present invention as a part of a computer system.

FIG. **2** is a more detailed block diagram of an embodiment of the integrated multimedia encoding system of the present invention.

FIG. **3** is a more detailed block diagram of a multimedia encoder in accordance with the present invention.

FIG. **4** is a more detailed block diagram of an adjustable delay engine in accordance with the present invention.

FIG. **5** is a more detailed block diagram of an embodiment of a memory allocator and unified memory module in accordance with the present invention.

FIG. **6** is a block diagram of an embodiment of allocatable memory buffers in accordance with the present invention.

FIG. **7** is a more detailed block diagram of an embodiment of a stream processor and multimedia processor in accordance with the present invention.

FIG. **8** is a flow chart illustrating a method of optimizing bit rates in a multimedia encoding system in accordance with the present invention.

FIG. **9** is a flow chart further illustrating the method of FIG. **8**.

FIG. **10** is a flow chart further illustrating the method of FIG. **8**.

FIG. **11** is a flow chart illustrating a method of storing data in a unified memory module in accordance with the present invention.

FIG. **12** is a flow chart illustrating a method of allocating blocks in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** illustrates a computer system **100** having an integrated multimedia encoding system **120** to perform video, audio, and other encoding tasks. In the MPEG or MPEG2 formats, video and audio data is encoded by a multimedia encoder and multiplexed to generate a program

or transport stream. The program or transport stream is then transmitted to a remote device which decodes the data to enable a user to see or hear the information content. The computer system **100** has a central processing unit **104**, which may execute specific programs related to multimedia processing, or may only perform other unrelated functions in an embodiment where the integrated multimedia encoding system **120** has a separate Digital Signal Processing (DSP) core. The CPU **104** is coupled to random access memory **116** and read only memory **128** on bus **122**. However, other computer architectures may be used in accordance with the present invention. A data source **108**, such as a CD-ROM, DVD-ROM, remote site, or a live source of multimedia data is coupled to the computer system **100** through bus **122**. The output of the integrated multimedia encoding system **120** is transmitted to a communications device **112** for transporting the encoded and multiplexed data or a storage medium **116** for storage of the program or transport stream data, or a decoder for decoding the data for playback. The system **100** may be implemented as a personal computer, or as an integrated part of a consumer electronics device, such as a video recorder or camera.

FIG. **2** illustrates the integrated multimedia encoding system **120** in more detail. Preferably, the present invention is implemented as a single-chip integrated multimedia encoding system **120**; however, the various components illustrated may also be implemented separately. Multimedia data **230** is transmitted to the integrated multimedia encoding system **120** from a data source **108** within computer system **100** or external to computer system **100**. The multimedia encoders **208** receive the data **230** and compress the data **230** responsive to the compression format being used in the computer system **100**, such as the MPEG2 compression standard. The encoders **208** perform conventional compression techniques to create macroblocks (4:2:0, 4:2:2, or 4:4:4 macroblocks in MPEG 2) from blocks of video data, and create the appropriate inter-picture coding required to compress the video data for transmission. Each individual block of video data is processed by the discrete cosine transform to obtain frequency coefficients, and the resulting block of frequency coefficients is quantized. Conventional techniques such as zig-zag scanning and run length coding may be performed by the encoders **208** to convert the quantized frequency coefficients into run-amplitude pairs. After compressing the data **230** and generating elementary multimedia streams, the encoders **208** adjust the data rate of the elementary multimedia streams responsive to a data rate feedback signal **212**, **214**. The adjusted elementary multimedia streams **216**, **218**, are transmitted to the unified memory module **204** and multimedia processor **250**.

The unified memory module **204** receives the adjusted elementary streams **216**, **218**, the output combined data **224** as well as data streams from other data sources **236**, such as from the PCI bus, through a conventional FIFO **244**. If the other data sources **236** are not designed to be able to adjust output data rates responsive to data rate feedback signals **212**, **214**, their data rates are still used in order to determine optimal rates for the encoders **208** to achieve an overall optimal data rate for the system **120** and their storage requirements are dynamically allocated within the unified memory module **204**. Preferably there are at least two data sources **236** whose data rates are adjustable. The unified memory module **204** dynamically allocates blocks of memory to each stream responsive to memory allocation signal **220**, generated by multimedia processor **250**. Multimedia processor **250** is preferably a Digital Signal Processing (DSP) core which is designed to perform conventional

multimedia operations as well as the specialized functions in accordance with the present invention. The adjusted elementary multimedia streams **216**, **218** are also transmitted to the multimedia processor **250**, which monitors the data rates of the adjusted elementary multimedia streams **216**, **218** to generate the data rate feedback signals **212**, **214**. The stream processor **200** monitors the actual data rate of the combined multimedia stream **224** and transmits this data to the multimedia engine **250**. Finally, the stream processor **200** retrieves data on data line **240** from the unified memory module **204** and processes the data in accordance with a linked list of commands comprising dedicated instructions for multiplexing the data into a single output stream **224**. The combined stream data **224** is stored back into the unified memory module **204**. Bus **122** is used to access the combined stream data **224** for transmission to other components of the system **100**.

FIG. **3** is a more detailed block diagram of one embodiment of the multimedia encoder **208** in accordance with the present invention. Compression engine **312** encodes incoming video frames **230** into a video elementary stream or audio samples **230** into an audio elementary stream. The output compressed elementary multimedia stream **316** is transmitted to an adjustable delay engine **300**. The adjustable delay engine **300** adjusts the data rate of the compressed elementary multimedia stream **316** responsive to the data rate feedback signal **212**, **214** received from the multimedia processor **250**. The adjusted elementary multimedia streams **216**, **218** are transmitted to the unified memory module **204**.

FIG. **4** is a block diagram illustrating in more detail one embodiment of the adjustable delay engine **300**. The data rate feedback signals **212**, **214** are transmitted to a control unit **404** which controls the data rate of the compressed multimedia stream **316**. If the data rate must decrease, the control unit **404** enables the corresponding number of delay buffers **400** to produce a data rate which matches the target rate **212**, **214**. If the data rate of the compressed multimedia stream **316** must increase, delay buffers **400** which are currently enabled are disabled to increase the data rate of the elementary stream **316**. If the target data rate **212**, **214** and the analyzed data rate are equal, then the control unit **404** performs no operation, and the current data rate is maintained. In an alternate embodiment, the number of bits allocated for each macroblock, frame, or group of frames is adjusted by the control unit **404** in order to increase or decrease the data rate of the stream **316** described in more detail below. In a further embodiment, a conventional encoder is used as encoder **208**, and the multimedia engine **250** adjusts the data rate output of the encoder **208** by adjusting the rate of the data which is input to the encoder **208**, responsive to its analysis of the difference between the system data rate and the target data rate, also described in more detail below.

FIG. **5** illustrates a more detailed block diagram of an embodiment of a memory allocator **512** and unified memory module **204** in accordance with the present invention. Memory allocator **512** is part of the multimedia processor **250**; however, an independent processor may also be used to provide the allocation functions. Memory allocator **512** receives the adjusted elementary multimedia streams **216**, **218** and the combined multimedia stream **224**. Memory allocator **512** determines the storage requirements of each stream, and allocates data buffers **500** correspondingly across lines **220**.

As shown in FIG. **6**, the buffers **500** store compressed multimedia data **216**, **218** and output combined data **224**. When a buffer **600** stores compressed multimedia data **216**,

218 it stores instructions 606 for processing the data 216, 218 and the data itself 216, 218. When a buffer 604 stores output combined data 224, and only the data 224 itself are stored. The storage buffers 500 are built as a linked list of buffers which are processed sequentially by the stream processor 200. When the multimedia processor 250 determines the proper allocation of buffers 500 to accommodate the different streams, the multimedia processor 250 modifies the linked list accordingly. After every frame is generated, the memory allocator 512 determines how may bits were generated for the frame. Then, a buffer 600 is allocated for to store the information. The buffers 600 are sequentially ordered, and once a first buffer 600 is filled, a second buffer 600 is allocated to store the next frame. Once all of the buffers 600 have been filled, the memory allocator 512 rotates back to the first buffer 600 to allocate the next frame of data. As the stream processor processes the buffers 600 in sequence, by the time the memory allocator 512 rotates back to the first buffer 600, the stream processor will be finished processing the information in that buffer 600. The allocator 512 is therefore able to dynamically allocate buffers 600 of different sizes to store incoming frames of different sizes, thus optimizing the use of the memory module 204 and increasing the overall efficiency of the system.

The instructions 606 for processing the adjusted elementary multimedia streams 216, 218 are preferably dedicated instructions written into the buffers 600 for the stream processor 200 to access and execute. The instructions 606 are written into the buffers 600 by the multimedia processor 250. Using dedicated instructions allows the programmer to easily manipulate the data with confidence that the intended operations are performed accurately. Also, dedicated instructions 606 are more efficient as they are tailored to the precise operations required in stream multiplexing. In an exemplary embodiment, the instructions 606 include program control instructions, data access instructions, and data processing instructions. Program control instructions include NOP, STOP, JUMP, INTERRUPT. Data access instructions include READ and WRITE instructions for reading and writing data to and from memory 204. The data processing instructions are specific for the data manipulations required to multiplex the adjusted elementary multimedia streams 216, 218 and generate the combined multimedia stream 224. These include START_STOP_CRC, which is used to delimit data included in a checksum calculation, INSERT_CRC, which inserts the computed CRC into the data stream at the current position, INSERT_TIME_STAMP, which causes the current time stamp to be inserted at the current position, STUFF, which inserts a programmable number of bits into the combined multimedia stream 224, and ENCRYPT, which performs encryption on the associated data, according to the DVD or DVB encryption requirements.

The use of dedicated instructions 606 with a programmable stream processor 200 allows the system 120 to provide a high level of granularity in performing its multiplexing operation. The multimedia processor 250 is capable of determining whether a stream is an elementary stream, program stream, or transport stream, all of which must be formatted differently, and is capable of determining the byte size used in a current stream. The multimedia processor 250 is then able to tailor the instructions 606 to adjust the multiplexing of the programmable stream processor 200 and also adjust the data rates of the stream to optimally process the data responsive to the format required. In conventional systems in which the multiplexing operation is hard-wired to an unresponsive CPU, the multiplexing operation was not able to adjust for different formats. Rather, one ratio must be used to accommodate all formats, and no control over the byte sizes of the data is provided. A predetermined ratio, because of its general applicability, is not optimal for processing streams which may be of multiple formats, and cannot be tailored to meet the real time requirements of the system. In contrast, the programmable stream processor 200 in accordance with the present invention is able to process the data at a fine level of granularity in accordance with the intended format of the stream and the current system requirements.

FIG. 7 is a more detailed block diagram of an embodiment of the stream processor 200 and multimedia processor 250 in accordance with the present invention. The stream processor 200 includes MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined multimedia stream 224. Combined multimedia stream 224 is preferably a program or transport stream as specified in MPEG2. The MUX logic 750 accesses the unified memory module 204 through data line 240 to retrieve the data and the instructions to perform on the data. After performing the required operations, the data 224 is temporarily written back to memory 204, for later transfer to the communications device 112 or other recipient of the Program or Transport Stream 224.

The stream processor 200 also comprises a data rate analyzer 700 which analyzes the data rate of the combined multimedia stream 224 to generate data rate value 710. The data rate is analyzed by computing the number of bits transmitted over a given period of time. The use of the actual data rate of the combined multimedia stream 224 provides a very accurate determination of whether and what adjustments should be made to the encoders 208 to maintain the optimal data rate of the system 120. In one embodiment, a second data rate analyzer 724 in the multimedia processor 250 analyzes the adjusted elementary multimedia streams 216, 218 to determine the data rates 706, 708 by dividing the number of macroblocks, frames, and groups of frames stored in the memory by the number of bits used in the macroblocks, frames, and groups of frames. The data rate 706, 708 of an elementary multimedia video stream is determined by analyzing the number of bits allocated up to a previous macroblock which has been sent. For an audio elementary video stream, the bit rate is measured per frame. However, one of ordinary skill in the art is aware of multiple methods for determining a data rate of an elementary multimedia stream 316 in accordance with the present invention. In a preferred embodiment, a data rate 706, 708 is computed for every four or five frames, and the number of bits in a macroblock, frame, or group of frames is used to determine the data rate 706, 708. The number of bits in a macroblock is determined by the quantization number (Q) as is known in conventional MPEG techniques. In one embodiment, the data rate analysis is performed by the encoders 208. In an alternate embodiment, the adjusted elementary multimedia streams 216, 218 are also analyzed by the stream processor 200 to generate actual data rate values 706, 708.

The actual data rate 710 of the system 220 is transmitted to the multimedia processor 250 and compared to a target data rate 226 of the system 120 by a data rate comparator 716. The target data rate 226 of the system 120 is transmitted to the integrated multimedia encoding system 120 from a user or other source to dictate the optimal or maximum throughput of the system 120. The target data rate 226 is preferably adjustable as the system's needs and capabilities

change and is input to either the multimedia processor **250** or the stream processor **200**, for transmittal to the data rate comparator **716**. The data rate comparator **716** generates a rate recommendation control signal **734** to indicate whether the system **120** is operating below, at, or above the maximum or target throughput **226**.

The data rates **706**, **708**, and the control signal **734** are then transmitted to a data rate optimizer **704** in the multimedia processor **250**. The data rate optimizer **704** generates data rate feedback signals **212**, **214** to ensure that the actual data rate **710** of the system **120** approximates the target data rate **226** of the system **120**. Responsive to the rate recommendation control signal **734** indicating that the system throughput **710** is less than the target rate **226**, the data rate optimizer **704** generates rate control or data rate feedback signals **212**, **214** indicating that one or both encoders **208** should increase their data rates, if possible. As described above, this is accomplished by disabling existing delays, increasing the rate at which data is fed into the encoders **208**, or increasing the number of bits per macroblock, frame, or group of frames. If the encoders **208** are already generating data at their maximum capabilities, then the system's throughput will remain below optimal until data is transmitted to the encoders **208** at a faster rate. In an embodiment in which multimedia processor **250** controls the rate at which data is fed to the encoders **208**, the processor **250** will adjust the rate at which data is input to the encoders **208** to increase the system throughput.

If the rate recommendation control signal **734** indicates that the system throughput **710** is above the target rate **226**, the data rate optimizer **704** generates rate control or data rate feedback signals **212**, **214** indicating that one or both encoders **208** should decrease their data rates. As described above, this is accomplished by inserting delays, decreasing the rate at which data is fed into the encoders **208**, or decreasing the number of bits per macroblock, frame, or group of frames. In one embodiment, an estimation engine within multimedia processor **250** determines whether an adjustment to one stream will raise the system throughput **710** to equal the target rate **226**. If the adjustment does not suffice to cause the system throughput **710** to equal the target rate **226**, then the data rates of the other streams are increased until the estimation engine determines that the estimated data rate equals the target rate **226**, and then data rate feedback signals **212**, **214** representing the final values are sent to the encoders **208**. The data rates of the streams may be adjusted in any order without affecting the efficacy of the present invention. In an alternate embodiment, the data rates of the adjusted elementary multimedia streams **216**, **218** are adjusted incrementally using loop feed back principles until the output data rate **710** equals the target rate **226**. In a further embodiment, the multimedia processor **250** instructs the stream processor **200** to stuff bits into the stream **224** using a STUFF command to adjust the data rate of the output stream **224** to the optimal or target rate. The above components **700**, **704**, **716**, **724** may be implemented as ASICs designed for the specific tasks described above as a part of the stream processor **200**, or may be implemented as modules designed to run by the multimedia processor **250**. Although the above embodiment has been described using only three streams **216**, **218**, **220**, the multimedia processor **250** is capable of analyzing and adjusting for any number of different streams of data required to be processed through the system **120**.

FIG. **8** is a flow chart illustrating a method of optimizing bit rates in a multimedia encoding system **120** in accordance with the present invention. First, the adjusted elementary multimedia streams **216**, **218** are combined **800** together into an combined multimedia stream **224**. Next, the data rate **710** of the combined multimedia stream **224** is determined **804**. The system determines **808** whether the data rate **710** of the combined multimedia stream **224** exceeds the target data rate **226**. If it does not, the method as described in FIG. **9** is performed. If it does, the method as described in FIG. **10** is performed.

Referring to FIG. **9**, the system determines **900** whether a nominal data rate of the first adjusted elementary multimedia stream **216** exceeds the current data rate **708** of the first adjusted elementary multimedia stream **216**. The nominal data rate is used in this embodiment to specify a target data rate for each adjusted elementary multimedia stream **216**, **218**. The target rate is chosen by a user or other source to specify a maximum data rate for the stream. If the nominal data rate of the first adjusted elementary multimedia stream **216** stream exceeds its actual data rate **708**, the data rate of the first adjusted elementary multimedia stream **216** is increased **904** to the nominal rate. If the nominal data rate does not exceed the actual rate **708**, the system determines **908** whether the next streams' nominal data rate exceeds its actual data rate. If it does, the data rate of the next stream is increased **912**. This process continues until all streams which are capable of having their data rates adjusted have been adjusted to their nominal rate.

FIG. **10** illustrates the methodology when the actual data rate **710** exceeds the target data rate **226**. This can occur due to inherent skew between the clock and data cycles. Although the amount of the overshoot may be small, if the overshoot is allowed to accumulate, the error may be significant. The data rate **708** of the first adjusted elementary multimedia stream **216** is compared **1000** to its nominal data rate. If the system determines **1004** that the data rate exceeds the nominal data rate, the data rate of the first adjusted elementary multimedia stream **216** is reduced **1008**. As described above, the rates are reduced by either adding a delay or decreasing the number of bits assigned to a macroblock, frame, or group of frames. If the data rate of the first adjusted elementary multimedia stream **216** exceeds the nominal rate, the next adjusted data stream is compared **1012** to its nominal rate. If the data rate of the next or Nth adjusted data stream exceeds its nominal data rate, the data rate of the Nth stream is reduced **1020**. Otherwise, the data rate of the last adjusted data stream is reduced **1024**.

FIG. **11** is a flow chart illustrating a method of storing data in a unified memory module **204** in accordance with the present invention. First, a number of blocks required for storing received audio, video, and combined data is determined **1100**. Next, the system determines **1104** whether the number of blocks required for storing audio data exceeds the number of currently allocated blocks in unified memory module **204**. If it does, more blocks in the unified memory module **204** are allocated **1120** to store audio data. If not, the system determines **1108** whether the number of blocks required for storing video data exceeds the number of currently allocated blocks. If it does, more blocks are allocated **1124** for storing video data. Then, the system determines **1112** whether the number of blocks required for storing the combined output multimedia data **224** exceeds the number of currently allocated blocks. If it does, more blocks are allocated **1128** for storing the combined data. If the current allocations are sufficient, the system retains **1116** the current allocations. In an embodiment in which other data streams are stored in unified memory module **204**, blocks are allocated in a similar manner.

FIG. **12** is a flow chart illustrating a method of allocating blocks in accordance with the present invention. FIG. **12**

illustrates a method for allocating audio blocks **1120**, but is applicable for allocating any blocks of memory to a data stream in accordance with the present invention. First, the system determines **1200** whether the number of blocks currently allocated for storing video data exceeds the number of currently required for storing video data. If it does, blocks which are currently allocated to store video are allocated **1208** to store audio data. Then, the system determines **1212** whether more blocks are required for storing the audio data. If there are more blocks required, the system determines **1204** whether the number of currently allocated blocks for the combined output multimedia data **224** exceeds the number of blocks required for storing the combined output multimedia data **224**. If it does, then blocks currently allocated to store the combined data are allocated **1216** to store the audio data. If no blocks are available to be allocated, an error message is generated. In an embodiment with other data streams, the other data streams are analyzed in a similar manner, where current allocations are compared with current requirements to determine whether more blocks are required or whether existing blocks can be reallocated.

While the present invention has been described with reference to certain preferred embodiments, those skilled in the art will recognize that various modifications may be provided. These and other variations upon and modifications to the preferred embodiments are provided for by the present invention.

What is claimed is:

1. In a system for combining input multimedia data streams to form an output multimedia data stream, an apparatus for adjusting rates of the input multimedia data streams comprising:

a data rate analyzer, coupled to the output multimedia data stream, for determining the data rate of the output multimedia data stream; and

a multimedia processor, coupled to the data rate analyzer, for comparing the determined output multimedia data stream data rate to a target output data stream data rate, and generating rate control signals for adjusting the data rates of the input multimedia data streams responsive to the comparison.

2. The apparatus of claim **1** wherein the multimedia processor further comprises:

a rate comparator, having a first input for receiving a target output data stream data rate and a second input coupled to the output of the data rate analyzer, for generating a rate recommendation signal;

a data rate optimizer, having a control input coupled to the rate comparator for receiving the rate recommendation signal, and generating rate control signals to be used by encoders to alter the data rates of the input multimedia data streams responsive to the rate recommendation signal.

3. The apparatus of claim **2** wherein the multimedia processor further comprises:

a data rate analyzer, having inputs for receiving compressed multimedia data of the data streams and outputs coupled to the data rate optimizer, the outputs defining a data rate for compressed multimedia data of the data streams; and

wherein the data rate optimizer analyzes the data rates of the compressed multimedia streams and the rate recommendation signal to generate rate control signals.

4. The apparatus of claim **1** wherein the input multimedia data stream is a video elementary stream.

5. The apparatus of claim **1** wherein the output multimedia data stream is a program stream.

6. The apparatus of claim **1** wherein the output multimedia data stream is a transport stream.

7. In a device for providing compression to input multimedia data streams, combining the compressed multimedia data streams into an output combined multimedia data stream, and storing compressed multimedia data streams and output combined multimedia data streams, an apparatus comprising:

at least one multimedia data encoder, comprising:

a compression engine, for compressing a multimedia data stream and providing a compressed multimedia data stream output; and

a data rate adjuster, coupled to the output of the compression engine, for adjusting the data rate of the compressed multimedia data stream output responsive to a rate control signal generated by a multimedia stream control unit;

a unified memory module, comprising:

a plurality of reallocatable multimedia data buffers;

a memory allocator, coupled to the multimedia data stream buffers, for determining storage requirements of the compressed multimedia data stream and the output multimedia data stream as the streams are received, and allocating buffers responsive to the determined storage requirements;

the multimedia stream control unit being coupled to the unified memory module and the multimedia data encoder, and comprising:

a data rate analyzer, coupled to the output combined multimedia data stream, for determining the data rate of the output combined multimedia data streams;

and a data rate feedback adjuster, coupled to the data rate analyzer and the at least one multimedia data encoder, for comparing the determined output combined multimedia data stream data rate to the target output combined data stream data rate, generating rate control signals for adjusting the data rates of the compressed multimedia data streams responsive to the comparison, and transmitting the rate control signals to the at least one multimedia data encoder.

8. The apparatus of claim **7** wherein the buffers comprise an instruction part and a data part, and the instruction part comprises at least one of a set of instructions for directing the multimedia stream control unit to perform data manipulations on information in the data part.

9. The apparatus of claim **8** wherein the instruction set includes program control instructions, data access instructions and data processing instructions.

10. The apparatus of claim **8** wherein the buffers are organized using link lists, and the buffers are accessed in accordance with the link lists.

11. The apparatus of claim **7** wherein there are two multimedia data encoders, a first encoder for encoding video data and a second encoder for encoding audio data.

12. The apparatus of claim **7** wherein the multimedia stream control unit comprises a target data rate input for receiving a target output combined multimedia data stream data rate.

13. A method for generating a combined multimedia data stream output having a data rate within a tolerance of a target data rate, in a device having multimedia encoders for generating encoded data streams and a data stream multiplexer, comprising the steps of:

combining the encoded data streams to form a single output data stream;

determining the data rate of the combined output data stream;

comparing the determined data rate to a target data rate;

responsive to the target data rate exceeding the determined data rate, adjusting the data rates of the encoded data streams until the combined output data stream data rate is within a tolerance of the target data rate; and

responsive to the determined data rate exceeding the target data rate, adjusting the data rates of the encoded data streams until the combined output data stream data rate is within a tolerance of the target data rate.

14. The method of claim **13** further comprising the step of:

monitoring the data rate of the encoded data streams;

wherein the responsive to the determined data rate exceeding the target data rate, adjusting the data rates step further comprises

comparing the monitored data rates of the encoded data streams to nominal data rates for the encoded data streams;

responsive to a data rate of an encoded data stream exceeding its nominal data rate, reducing the data rate of the encoded data stream; and

wherein the responsive to the target data rate exceeding the determined data rate, adjusting the data rates step further comprises:

comparing the monitored data rates of the encoded data streams to nominal data rates for the encoded data streams;

responsive to a nominal data rate of an encoded data stream exceeding the data rate of the encoded data stream, increasing the data rate of the encoded data stream.

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